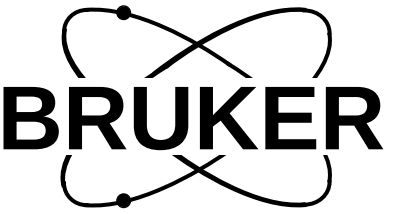

AQR

Router / Combiner
Router / Combiner -E

Service Manual

Index 004

BRUKER

This manual was written by

Max Erick Busse-Grawitz

Modified for BASH 2.0 by U. Roos - December 1996

Fällanden, Switzerland

P/N: Z31215
DWG-Nr: 882004

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General description 1

Introduction 1.1

The AQR Router/Combiner serves for routing signals from different inputs to different outputs and for combining them if needed (see ***"Operation"*** below).

There are two versions:

- Router/Combiner (standard frequency range)
- Router/Combiner -E (extended frequency range)

See ***"Technical Data" on page 23*** for further details on the above mentioned versions of the Router.

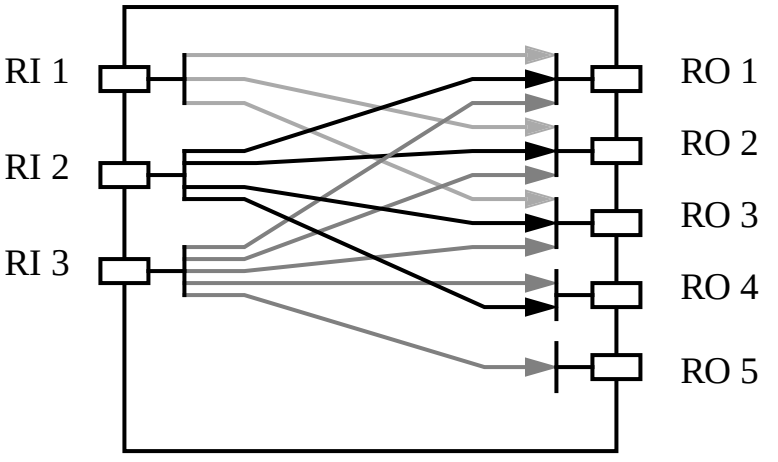
Features 1.2

- Mounted in 19’ HF moulded cases
- Computer controlled Routing/Combining
- Flat frequency response from 5...750 MHz
- Extended frequency range (up to 960 MHz) for Router/Combiner -E
- Good crosstalk and isolation characteristics
- I2C Bus

Operation 1.3

The figure below shows all routing/combining possibilities.

Figure 1.1. Routing/Combining possibilities



All routing/combining paths are set with the control input signals generated from the TCU unit.

The following chapter describes these control input signals for the PLD to set the switches in accordance to the desired routing/combining.

Control Input Signals *1.4*

The RSEL_xx (Routing Selection) signal group sets the path from the desired input RIx to the output ROx. The BLNK_TRx (Blanking) signal group enables the output.

Table 1.1. Control-Input Signals (PLD)

Direct Routing Input > Output (1-channel only)		Input-Section Switches			Output-Section Sw.	
		!RSEL_13 !RSEL_12 !RSEL_11 !RSEL_10	!RSEL_23 !RSEL_22 !RSEL_21 !RSEL_20	!RSEL_33 !RSEL_32 !RSEL_31 !RSEL_30	BLNK_TR1 BLNK_TR2 BLNK_TR3 BLNK_TR4 BLNK_TR5	
Input	Output [a]					
RI 1 (X_IN)	RO 1	1 1 1 0			0 1 1 1 1	
	RO 2	1 1 0 1			1 0 1 1 1	
	RO 3	1 1 0 0	1 1 1 1	1 1 1 1	1 1 0 1 1	
	RO 4	*1 0 1 1*			*1 1 1 0 1*	na[b]
	RO 5	*1 0 1 0*			*1 1 1 1 0*	na
RI 2 (H_IN)	RO 1		1 1 1 0		0 1 1 1 1	[e]
	RO 2		1 1 0 1		1 0 1 1 1	
	RO 3	1 1 1 1	1 1 0 0	1 1 1 1	1 1 0 1 1	
	RO 4		1 0 1 1		1 1 1 0 1	
	RO 5		*1 0 1 0*		*1 1 1 1 0*	na

Direct Routing Input > Output (1-channel only)		Input-Section Switches			Output-Section Sw.	
Input	Output [a]	!RSEL_13 !RSEL_12 !RSEL_11 !RSEL_10	!RSEL_23 !RSEL_22 !RSEL_21 !RSEL_20	!RSEL_33 !RSEL_32 !RSEL_31 !RSEL_30	BLNK_TR1 BLNK_TR2 BLNK_TR3 BLNK_TR4 BLNK_TR5	
RI 3 (Y_IN)	RO 1	1 1 1 1	1 1 1 1	1 1 1 0	0 1 1 1 1	
	RO 2			1 1 0 1	1 0 1 1 1	
	RO 3			1 1 0 0	1 1 0 1 1	
	RO 4			1 0 1 1	1 1 1 0 1	
	RO 5			1 0 1 0	1 1 1 1 0	
Example of combined signal routing:						
RI 1 + RI 2 > RO 2, RI 3 > RO 5 [c,d]		1 1 0 1	1 1 0 1	1 0 1 0	1 0 1 1 0	
					RO1 RO2 RO3 RO4 RO5	

a. The output ROx will be valid if the according output blanking signal BLNK_TRx is negated.

b. non available routing

c. In this example input RI1 should be combined with input RI2 and routed to output RO2. In addition to that, input RI3 should be routed separately to output RO5. The Control-Input signals have to be set as follows:

- the first selection signal group (!RSEL_1x = 1101) sets input RI1 to Output RO2
- the second selection signal group (!RSEL_2x = 1101) sets input RI2 to output RO2
- the third selection signal group (!RSEL_3x = 1010) sets input RI3 to output RO5
- the blanking signal group (BLNK_TRx = 10110) enables output RO2 and RO5

As an other example all inputs RI1-RI3 should be combined and routed to output RO3. In this case the Control-Input signals are: !RSEL_1x = 1100, !RSEL_2x = 1100, !RSEL_3x =1100 and BLNK_TRX = 11011.

d. for other combining/routing possibilities refer to schematics

e. built in option (ECL00)

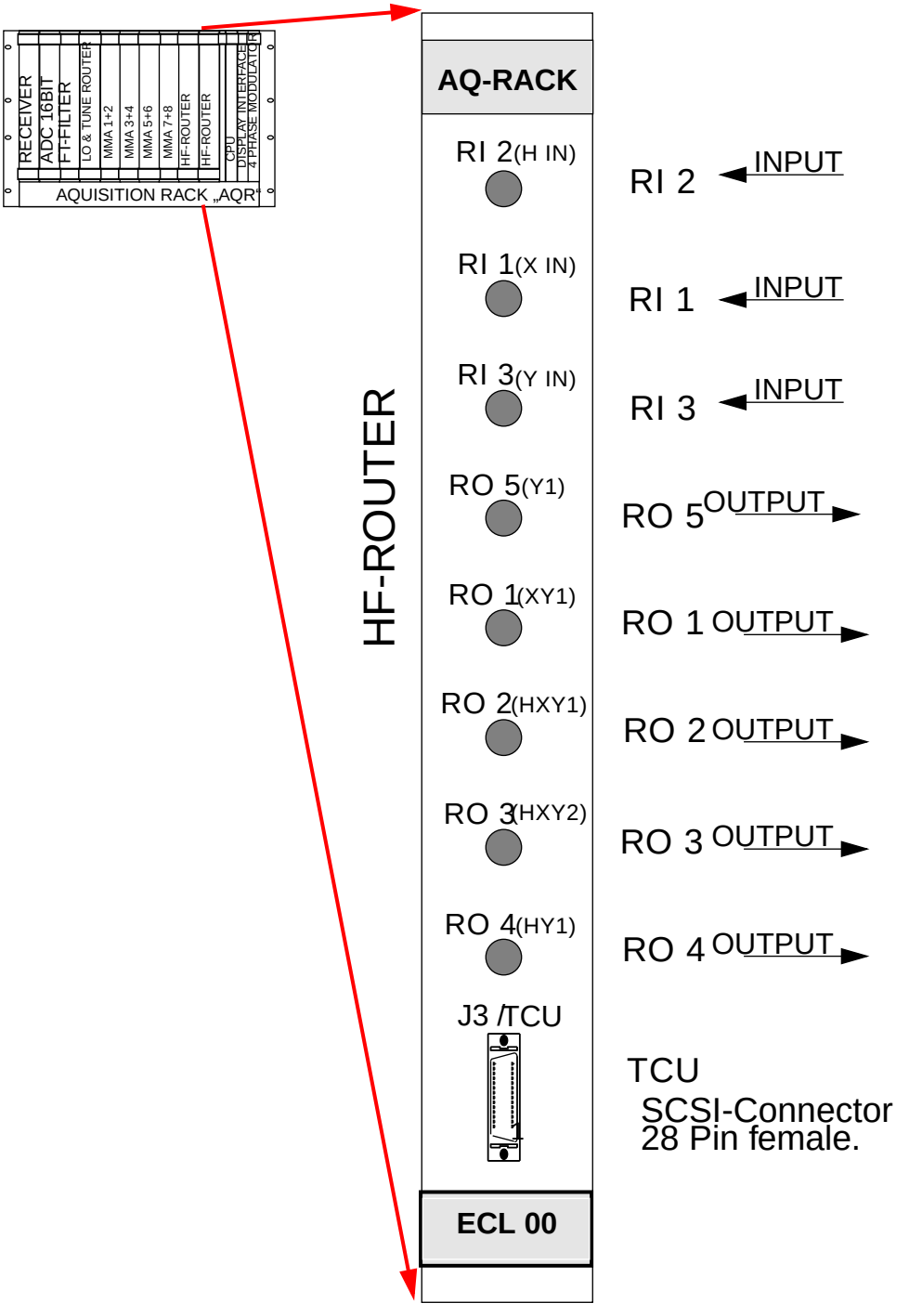
UXNMR Commands *1.5*

For the UXNMR command notation regarding the control input signals please refer to the UXNMR manual.

Connector Description 1.6

Front Panel 1.6.1

Figure 1.2. 3-Channel Router/Combiner Frontpanel



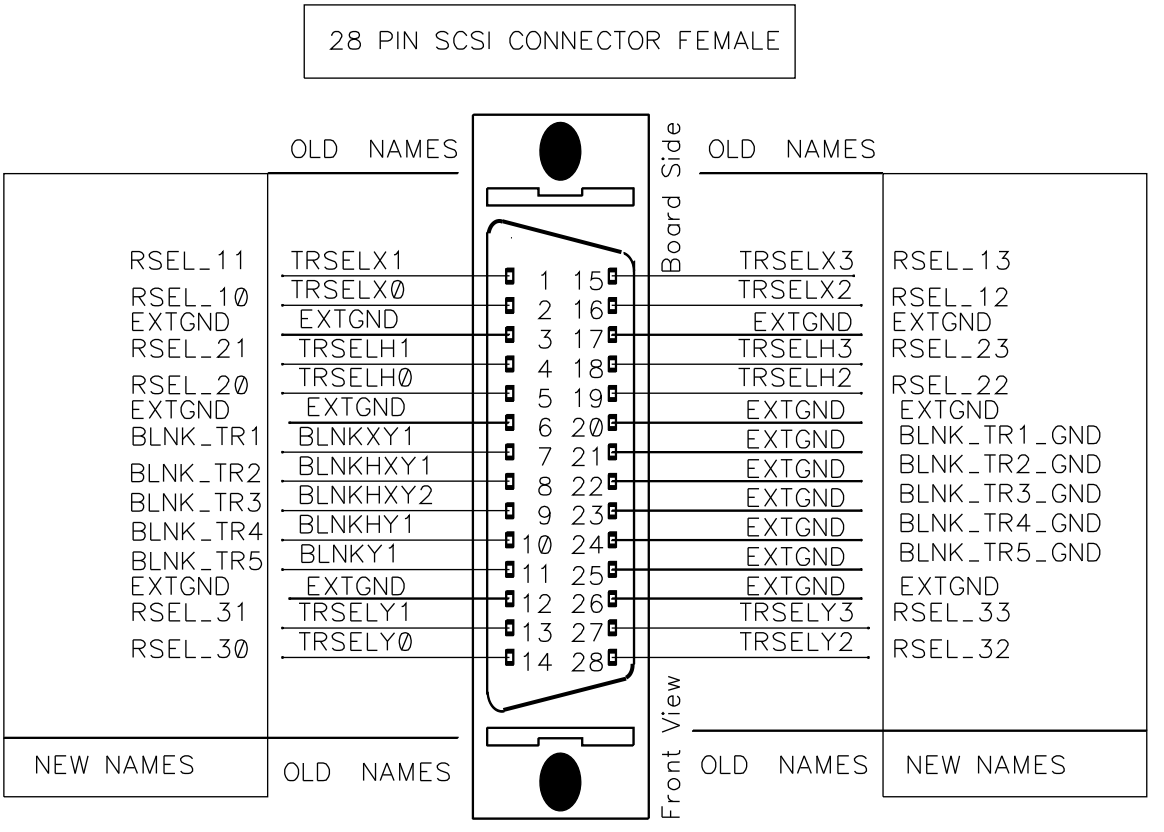
High Density SCSI Connector J3 1.6.2

The following Figure shows the wiring of the SCSI connector J3:

(The 28 pins should directly match pin 5 to pin 43 from the TCU connector T2)

Table 1.2. Signals on the High Density Connector J3

Figure 1.3. 3-Channel Router/Combiner: 28pin SCSI Connector



All inputs are driven from the TCU. The TCU-outputs are TTL-levels. They are in a high impedance state after power-on and pulled up by a resistor of 1kohm. The activated drivers are able to drive 32mA in „HIGH“ and 64mA at „LOW“.

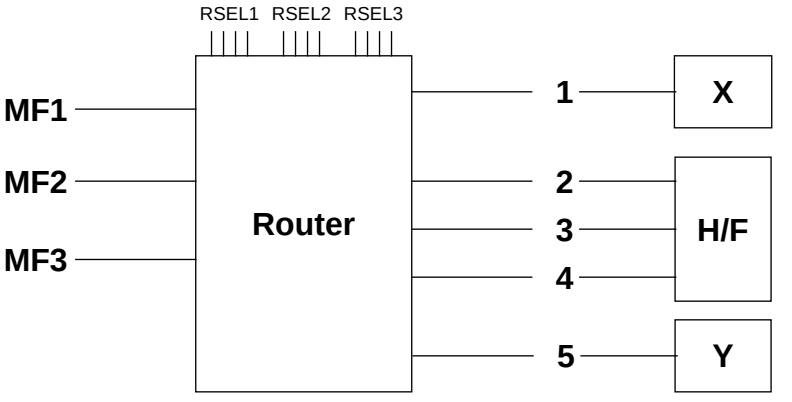
Configurations with one or more Routers 1.7

In this section, different possibilities to connect one or more routers to a spectrometer are described, according to the logic signal descriptions.

Configuration with one Router 1.7.1

A spectrometer with one router may be configured as follows:

Figure 1.4. Configuration with one router



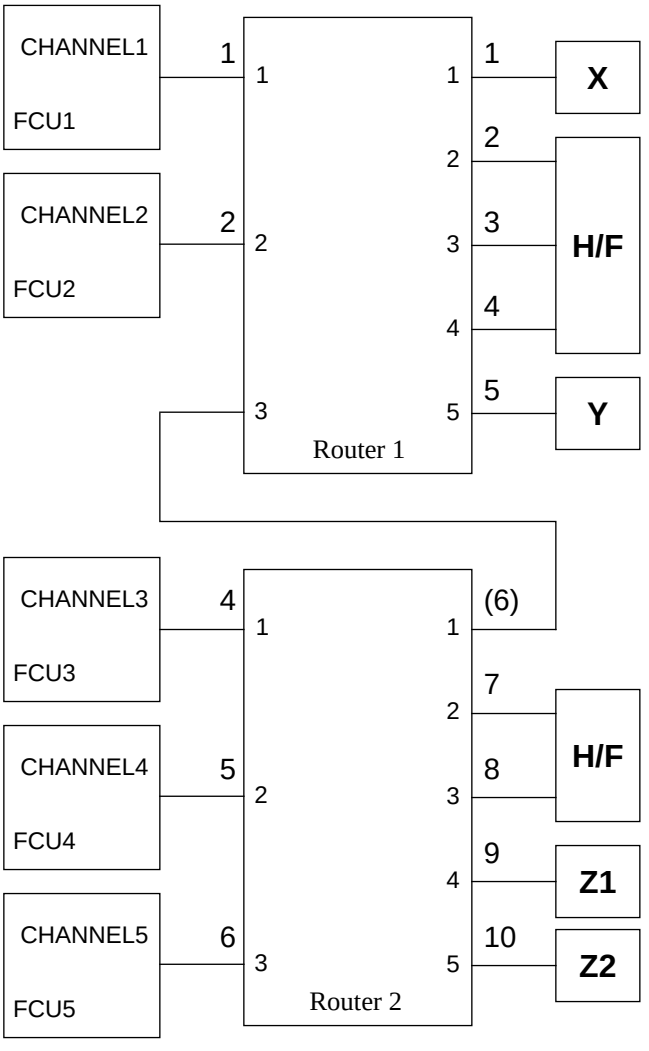
The router receives its signals from the TCU. The 50-pin SCSI connector of the TCU is connected to the router by a special 50 to 28 pin adaptor cable. The router is driven by the RSEL1x...3x and BLNK1...5 signals of the TCU.

Configuration with two Routers 1.7.2

Basically, nearly any configuration with two routers is possible. As with the single router configuration, the routers receive their signals from the TCU T2 50 pin SCSI connector. But now they are connected to it by a special Y adapter cable as described below. Each router receives its full set of digital signals, and all blanking signal for the routers are also available for the poweramps which will receive the router output signals. This means full flexibility in wiring FCUs and PAs to the routers. Each router has the same PLD, so if RSEL5 is set to 3, BLNKTR8 must be negated to route.

A typical configuration with two routers would look as follows:

Figure 1.5. DMX Configuration with two Routers



In this configuration, Router 1 is chained to Router 2, so all frequencies are available on Router 1. The PA blanking signal 6 remains unused and should be constantly deactivated (set to 0). Caution has to be taken when two routers are chained because the frequency characteristics of both routers are multiplied.

The Y Cable for a two router configuration

As mentioned above, there exists an Y cable (Cat_Nm Z002814) that links the TCU to two routers. The wiring list is included here for reference.

Table 1.3. Wiring of a configuration with two Routers

TCU.T2 (SCSI 50 pin)	Signal Name	Router 1 (SCSI 28 pin)	Router2 (SCSI 28 pin)
1	RSEL 51	-	4
2	RSEL 50	-	5
3	RSEL 61	-	13
4	RSEL 60	-	14
5	RSEL 11	1	-
6	RSEL 10	2	-
7	GND	3	3
8	RSEL 21	4	-
9	RSEL 20	5	-
10	GND	6	6
11	BLNKTR 1	7	-
12	BLNKTR 2	8	-
13	BLNKTR 3	9	-
14	BLNKTR 4	10	-
15	BLNKTR 5	11	-
16	GND	12	12
17	RSEL 31	13	-
18	RSEL 30	14	-
19	BLNKTR 6	-	7
20	BLNKTR 7	-	8
21	BLNKTR 8	-	9
22	BLNKTR 9	-	10
23	BLNKTR 10	-	11
24	RSEL 41	-	1
25	RSEL 40	-	2
26	RSEL 53	-	18

TCU.T2 (SCSI 50 pin)	Signal Name	Router 1 (SCSI 28 pin)	Router2 (SCSI 28 pin)
27	RSEL 52	-	19
28	RSEL 63	-	27
29	RSEL 62	-	28
30	RSEL 13	15	-
31	RSEL 12	16	-
32	GND	17	17
33	RSEL 23	18	-
34	RSEL22	19	-
35	GND	20	20
36	GND	21	-
37	GND	22	-
38	GND	23	-
39	GND	24	-
40	GND	25	-
41	GND	26	26
42	RSEL 33	27	-
43	RSEL 32	28	-
44	GND	-	21
45	GND	-	22
46	GND	-	23
47	GND	-	24
48	GND	-	25
49	RSEL 43	-	15
50	RSEL 42	-	16

Configuration with three Routers *1.7.3*

Configurations with three routers are not yet supported but planned to be possible. A configuration with three routers will be essentially the same as with two routers, i.e. all capabilities of the router will be available. There will be fifteen blanking pulses for the routers as well as for the power amplifiers, so each router output may be used to be chained to another router or as an output to an amplifier. Up to eight FCUs will be supported.

Functional description 2

Introduction

In this chapter the circuitry of the three channel router shall be described in a top-down approach.

The circuit consists of an input section with three similar divisions which is connected by switches to the output section consisting of five similar divisions. The switching is controlled by the control section.

The following table describes the logical structure of the routing and combining:

Table 2.1. Routing possibilities

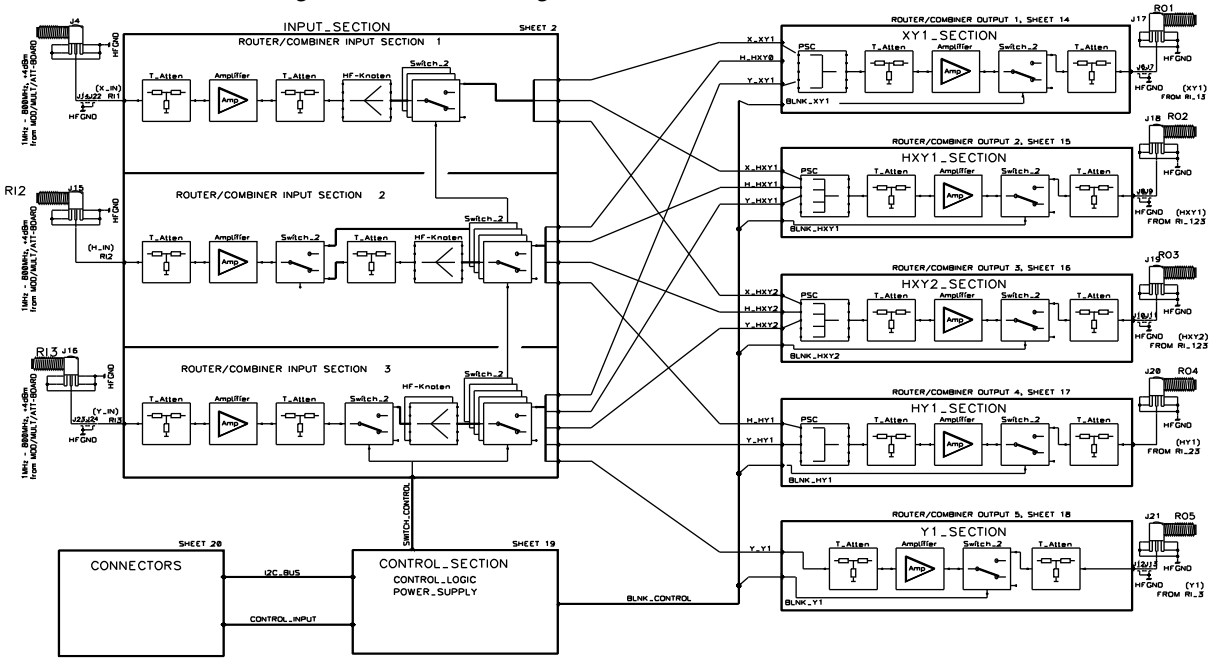
	OUTPUT				
INPUT	RO 1	RO 2	RO 3	RO 4	RO 5
RI 1	X	X	X	NP[b]	NP
RI 2	X[a]	X	X	X	NP
RI 3	X	X	X	X	X

a ECL00; built in option, ECL01; Integrated normal routing/combining path

b. NP = Not possible

Block Diagram 2.1

Figure 2.1. Block Diagram



Old Routing Path Names 2.1.1

Input and output ports were formerly named differently. The following table shows the origin of these old names which are still used on the schematics and therefore in the function descriptions of the different sections.

Table 2.2. Old routing path names

Input Names		Switches	Routing	Output Names	
new	old			old	new
RI 1	X_IN	X_XY1		XY1 (or HXY0)	RO 1
		X_HXY1			
		X_HXY2			
RI 2	H_IN	H_HXY0		HXY1	RO 2
		H_HXY1			
		H_HXY2		HXY2	RO 3
		H_HY1			
RI 3	Y_IN	Y_XY1			
		Y_HXY1			
		Y_HXY2		HY1	RO 4
		Y_HY1			
		Y1		Y1	RO 5

The Input Section *2.2*

The input section consists of three divisions numbered from one to three that were formerly named X, H and Y. The X section connects to three, the H section to four and the Y section to five different outputs. In its structure the X section is the simplest one. It shall therefore be described first.

The signal enters the input section through an SMA connector and passes an attenuator before it is amplified by an MSA with approx. 10.5dB gain. After a further attenuator it reaches a HF knot, where it is split and directed to three switch sections X_XY1, X_HXY1 and X_HXY2.

Each of these sections consists of three switches in a row. The first two are placed near the input section, the third near the output section. The separation is done to improve the crosstalk and isolation characteristics. The input section switches are connected to the output section switch by semiflexible coaxial cables or PCB-wires.

The Y section is similar to the X section. The only difference is that it contains an additional switch that selects one of two HF knots. One is leading to two, the other one to three output sections. Thus, all five outputs can be accessed by the Y section.

The H section is best described as an X section expanded by an additional H=>HXY0 routing path. ECL00 prints have this path built as an option on a ‘piggy

back' board, whereas ECL01 prints have it integrated onto the main board as a normal routing path.

The option consists of two switches and their corresponding networks.

The Output Section 2.3

The output section consists of five divisions, each corresponding to an output as shown in the block diagram. Each part contains a combiner for the incoming routing signals (except the Y (RO5) section), an attenuator, an MSA amplifier and a blanking switch.

The HXY1 (RO2) and HXY2 (RO3) sections have three inputs and combine their signals with a four-way power splitter/combiner (the fourth input of the power combiner is terminated).

The HY1 (RO4) section has two outputs and therefore combines the incoming signals with a two-way power combiner.

The HXY0 (RO1, former XY1) section formerly had only two inputs (as the HY1 section) and therefore contains a 2-way power combiner. The third input (coming from the H_HXY0 option) is combined resistively with the output of the power combiner. Because of different frequency characteristics of the option, the H_HXY0 signal passes an extra attenuator before being combined to the other signals.

The Control Section 2.4

The control section accommodates logic to control the router switching as well as a power supply diagnostic feature (PS_Control, sheet 22 of the schematics) accessible by the I2C bus that is wired to the backplane.

Router Switching Control

Router switching is controlled by the control signals as described in the function description chapter. Additionally, the whole switching may be disabled by using the spectrometer enable (INSPENAB~) signal. The decoding is done on an EP910 PLD. The logic is fully combinatorial; no clock is needed.

The decoding is done in such a manner that only simultaneous switching may occur, i.e. the switches of a routing path are either all open or all closed. This means that full isolation may be obtained by simply negating the blanking signal of the corresponding output. Thus, fast on/off toggling without the risk of glitches or hazards may be obtained by applying statically the router select (RSEL) signals and toggling the corresponding blanking signal.

Features accessible by the I2C Bus 2.4.1

The I2C bus permits access to a simple power diagnostic feature as well as to an EEPROM that is intended to contain service information (BBIS).

The I2C bus lines are wired to the backplane. Their names are SDA (serial data) and SCL (serial clock). The direction line SDIR is not required because optocouplers are not used on this board.

The I2C base addresses are 0x40 for the IO chip and 0xE0 for the EEPROM. To access the chips, twice the device address must be added to the base address. The remaining LSB indicates read/write.

The power diagnostic feature consists of an I2C IO chip and some analog circuits to detect power fail. The four power supplies are tested and wired as follows:

I2C power fail diagnostics

node name	wired to bit	fail on	fail value
+5V_HFR	0	out of range	LOW
-5V_HFR	1	short circuit	HIGH
+12V_HFRI	2	short circuit	LOW
+12V_HFRO	3	short circuit	LOW

BBIS

The Bruker Board Information System (BBIS) is also implemented in the Router. It contains concise information on its board version, ECL, basic capabilities etc. A dump of the actual BBIS (ECL02) with comments is given below. Note that details of this information may change without notice.

```
B 1     Block1          Productiondaten
V 2                     Version
C 1     R               Protokoll-Devicename (BoardId)
S 5     ROUT            Rufname
S 16    Z002496         Teile-Nr.
S 16    0416            Serie-Nr.
S 10    Z3P2933C        Print-Nr.
U 1     8               HW-Code
S 7     950210          Herstell-Datum
C 1     Z               Produktionsort
U 1     3               Abteilung
S 5     BUS             Pruefer
U 1     1               Pruefplatz
U 1     2               ECL-Herstellung
E 1                     End


B 2     Block2          Servicedaten
V 0                     Version
E 2                     End


B 3     Block3          Geraetedaten
V 0                     Version
U 1     3               InputChannel
U 1     5               OutputChannel
U 2     860             MHz
S 10    -2/+2.0         Gain[dB]
S 4     1.6             VSWR Input MAX
S 4     1.7             VSWR Output MAX
U 1     3               RI1->RO1 (Routing possibilities)
U 1     4               RI2->RO1 (Routing possibilities)
U 1     5               RI3->RO1 (Routing possibilities)
```

```
E 3                     End


B 4     Block4          Applikationsdaten
V 0                     Version
E 4                     End


E 5                     End
```

Technical Data 3

Table 3.1. DC Specifications for Router/Combiner and Router/Combiner -E

Characteristics		min.	typ.	max.	Unit
+15V supply current		400	480	550	mA
+9Vsupply current		210	230	280	mA
-9V supply current		150	160	260	mA

Table 3.2. AC Specifications for the Router/Combiner (standard frequency range)

Characteristics	ECL[a]	Frequency [MHz]	min.	typ.	max.	Unit
Isolation between Input and Output	00 01 02 03	5..750 5..860 5..960	45 60 60 70	60 70 70 80		dB dB dB dB
Crosstalk between two or three routed paths	00 01 02 03	5..750 5..860 5..960		-45 -60 -60 -65	-35 -45 -45 -50	dB dB dB dB
Transmission gain	00 01 02 03	10..750 10..860 10..960	- 2.5 - 2.0 -2.0 -2.0		+ 2.5 + 2.0 +2.0 +2.5	dB dB dB dB
Noise figure	00,01 02 03	10..750 5..860 5..960	10 10 10	14 14 14	18 18 18	dB dB

Characteristics	ECL[a]	Frequency [MHz]	min.	typ.	max.	Unit
P1dB[b]	00 01, 02 03	10	5.5 2.8 3.8			dBm dBm dBm
	00 01..03	200	5.2 8.2			dBm dBm
	00 01, 02 03	500	6.3 7.3 7.8			dBm dBm dBm
	00 01, 02 03	750	5.1 6.8 5.8			dBm dBm dBm
	03	960	4.2			dBm
Input VSWR	00 01 02 03	5..750 5..860 5..960		1.3 1.3 1.3 1.3	1.6 1.5 1.6 1.7	/ / /
Output VSWR	00, 01 02 03	20..750 5..860 5..960		1.3 1.3 1.3	1.7 1.7 1.8	/ /
Switching time on-> off (10%)[c]	all		60	75	95	ns
Switching time off->on (90%)	all		70	85	105	ns

a Refer to ***"ECL Information" on page 27*** for definition of engineering change levels.

b P1dB is here the input power at which the signal gain has decreased by one dB.

c This means that the rf signal is being switched off by asserting the appropriate blanking pulse. The time will be measured when the rf signal has decreased below 10% of its original amplitude.

Table 3.3. AC Specifications for the Router/Combiner -E (extended frequency range)

Characteristics	ECL[a]	Frequency [MHz]	min.	typ.	max.	Unit
Isolation between Input and Output	all	5..960	70	80		dB
Crosstalk between two or three routed paths	all	5..960		-65	-50	dB
Transmission gain	00 01	5..960 5..365 365..960	-2.0 0.0 -0.5		+2.5 +3 +3.5	dB dB
Noise figure	all	5..960	10	14	18	dB

Characteristics	ECL[a]	Frequency [MHz]	min.	typ.	max.	Unit
P1dB[b]	00 01	10	2.8 3.8			dBm
	00 01	200	6.7 8.7			dBm
	00 01	500	5.3 7.8			dBm
	00 01	750	5.8 6.8			dBm
	00 01	960	4.2 5.7			dBm
Input VSWR	all	5..960		1.3	1.7	/
Output VSWR	all	5..960		1.3	1.8	/
Switching time on-> off (10%)[c]	all		60	75	95	ns
Switching time off->on (90%)	all		70	85	105	ns

a Refer to ***"ECL Information" on page 27*** for definition of engineering change levels.

b P1dB is here the output power at which the signal gain has decreased by one dB.

c This means that the rf signal is being switched off by asserting the appropriate blanking pulse. The time will be measured when the rf signal has decreased below 10% of its original amplitude.

ECL Information 4

Router/Combiner (standard frequency range) 4.1

In the following table, the engineering changes for the Router/Combiner (Part. No. Z002496) are listed. Refer to ***"Technical Data" on page 23*** for further ECL information.

Table 4.1. ECL (Engineering Change Level) Information for the Router/Combiner

ECL	Additional Features or Changes	Print Index	PLD Software
Prototype	no H_HXY0 switch	Z3P2933	ART0AA01-ZE
ECL 00	H_HXY0 switch as ‘piggy back’ option	Z3P2933A	ART0AB01-ZE
ECL 01[a]	- H_HXY0 switch and I2C circuit integrated on mainboard - P1dB and gain flatness improved - Isolation and crosstalk improved	Z3P2933B[b] Z3P2933C	ART0AB01-ZE
ECL 02[c]	Freqency range extended to 860 MHz	Z3P2933C	ART0AB01-ZE
ECL 03[d]	Frequency range extended to 960 MHz, slightly changed specifications	Z3P2933D	ART0AB01-ZE

a currently produced Router/Combiner

b Print index B and C are identical (except for some minor layout changes). The schematics are the same.

c no longer produced

d This ECL has now become the Router/Combiner -E

Router/Combiner -E (extended frequency range) *4.2*

The Router/Combiner -E (Part. No. Z012496) sprang from the former ECL03 of the Router/Combiner and has now become a product itself. Refer to ***"AC Specifications for the Router/Combiner -E (extended frequency range)" on page 24*** for further ECL information.

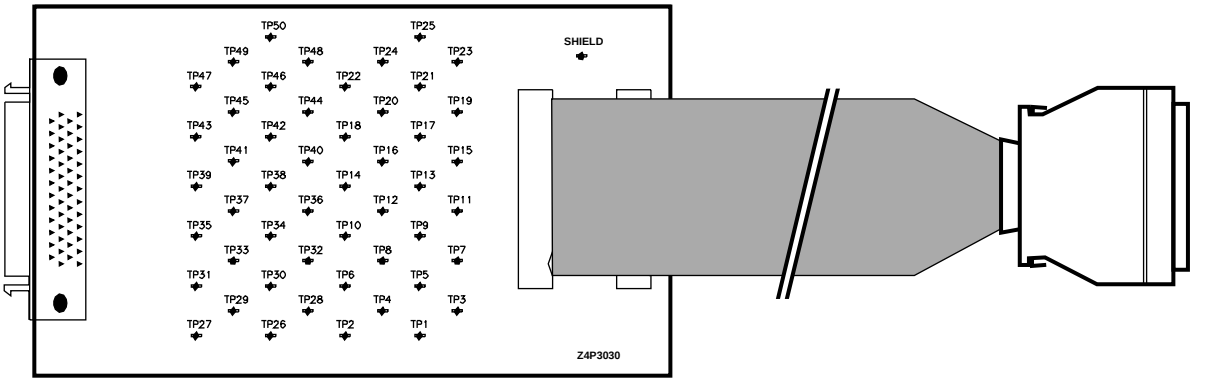
Table 4.2. ECL (Engineering Change Level) Information for the Router/Combiner -E

ECL	Additional Features or Changes	Print Index	PLD Software
ECL 00		Z3P2933D	ART0AB01-ZE
ECL 01	guaranteed positive gain for X nuclei up to 365 MHz	Z3P2933D	ART0AB01-ZE

Test Equipment 5

Avance Testadapter SCSI 50pol. 5.1

Figure 5.1. Avance Testadapter SCSI 50pol.



The SCSI 50pol. Avance Testadapter (Cat.Nm. Z002816) can be used to check the input control signals coming from the FCU.

To get an easy access to all signals, just plug this adapter between the FCU and the connecting cable to the 3-Channel Router/Combiner.

For the adapters test pin assignment please refer to the schematics or (in case of the Router Y-Cable) to the wiring list as shown on the table ***"Wiring of a configuration with two Routers" on page 14***.

Figures

Figures

Tables

Tables