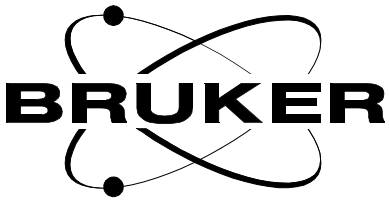


Communication Control Unit CCU 9/10

AQS/AQX
Technical Manual

Version 001

BRUKER

The information in this manual may be altered without notice.

This manual was written by

Jiri Tucek, Mirek Dudek

Rheinstetten, Germany

P/N: Z31561
DWG-Nr: 1273001

AQX CCU/9_4x00
AQS CCU/10_4x00

J. Tucek / M. Dudek

Contents

Figures

Tables

1. Starting with CU09/10

1. 1. Special features of CU09/10

CU09/10 provides the same devices and connectors as CU08 except the console connector which has been changed to the same type as on Indy (Mini D, 8 pin). Therefor, the CU08–Indy Console Cable can be used in reverse direction to connect CU09/10 to O2.

Additionally, there is the Fast Ethernet device with 2 RJ45 sockets. Only one of these sockets can be used at a time. Both sockets must not never be plugged but this would not result in any damage.

The standard Ethernet (10Base2 or so called Cheapernet) is available but can not be run by the ”unix 970501” included in ”xwin–nmr2.0”. A later version will manage both ethernet devices.

1. 2. Hardware Implementation

All CU09/10 connections can be carried out as on CU08 except the RS485 at CU10. The Cheapernet should be left unconnected.

The Fast Ethernet of CU09/10 is to be connected to the first or second ethernet interface on O2, the so called `ec0` or `ec1` (see workaround).
There are two RJ45 Fast Ethernet sockets on CU09/10. They are connected inside to the same signals but have crossed pin assignments.
The upper socket (signed ”FETH–HUB”) has to be used if CU09/10 will be connected to an HUB. This is the normal way with twisted pair ethernet hosts.
The lower socket (signed ”FETH HOST”) has to be used to connect CU09/10 by the same normal cable to another host (point–to–point connection).
That means, connect CU09 from socket ”FETH HOST” to the O2 by one of the following cables:

Cable Type	Category	Part Number	Length
UTP	CAT 5	83025	5m
UTP	CAT 5	83026	10m

You don’t need any longer the ”Mini Hub” (Part# O001114) that you might used to connect the O2 to the CU08.

The Console interface can be connected
to a Terminal by cable HZ04112 or
to the O2 by cable HZ04161.

The LINK Led (2. led from left in upper row) shows a good link status after power up. Otherwise one of the two link partners is down by software or power. The Fast Ethernet cable can be pulled out and plugged in under power and activity. Autonegotiation and link checking starts on both partners without software interaction if the link has been broken.
Unplugging, powering down or typing **`ifconfig ec1 down`** on O2 or
`ifconfig fen down` on `spect` break the link.

Exception with Indy

Attach the Fast Ethernet cable to the BNC Cheapernet connector via an
10BaseT ”Mini Hub”, Part# O001114 or

replace the AUI/10Base2 ”Micro Transceiver” by an
AUI/10BaseT ”Micro Transceiver”, Part# O00744
which fits to the cable.

The Fast Ethernet will adjust itself to the 10 MHz speed of the Indy.

The console interface of CU09/10 can be connected to the Indy by the
Console cable Part# HZ10091.

Exception with Aspectstation

Attach the Fast Ethernet cable to the BNC Cheapernet connector via an
10BaseT ”Mini Hub”, Part# O001114.

The Fast Ethernet will adjust itself to the 10 MHz speed of the Aspectstation..

The console interface of CU09 can be connected to the Aspectstation by the
Console cable Part# Hz04161.

1. 3. Software Implementation

Fast Ethernet needs the `unix 970501` included in `xwin–nmr2.0` or later.

The ethernet address of the exchanged CU08 has to be cleared on the O2 by typing

```
arp –d spect
```

Suggestion

If you, nevertheless, meet problems in booting the `spect` and before you try it again, you should expect the O2 (`ec0` or `ec1`) to be in an undefined state and type:

```
ifconfig ecx down
ifconfig ecx up
```

depending on the interface to which the `spect` is connected to.

1. 4. Problems of Point–to–Point Connection to the O2

Both link partners of a Fast Ethernet Connection exchange their abilities (10 or 100 MBit and Half or Full Duplex) after power up and without software interaction. They decide then for the fastest common possibility. This procedure is called Autonegotiation respectively Parallel Detection.

The main interface of the O2 is only able to operate in Half Duplex and behaves like an Hub. The secondary interface is ready for Full Duplex but there is no software support for this on O2. The CU09/10 is able to run Half and Full Duplex.

This situation leads to an improper mode decision and to a Full Duplex link at the secondary interface which can’t work.
To ensure an Half Duplex decision, the Full Duplex mode is switched off on CU09/10 by software. This decreases the performance by at least 10 % and leads to collisions.

Furthermore, the point–to–point connection with O2 causes errors during the boot sequence.
This problem can be solved by connecting the O2 to the CU09/10 via an Hub or by connecting the CU09/10 to the main interface of the O2 (which behaves like an Hub).

Workaround

Swap logically both ethernet devices of the O2. That means, connect the `spect` to ethernet controller `ec0` on the motherboard of the O2. This can easy be carried out by modifying the file `netif.options`.

Type on O2 as superuser:

```
vi /etc/config/netif.options
```

This file contains the 2 parameter entries of `if1name=ec0` and `if2name=ec1`. Swap the values of both parameters to:

```
if1name=ec1
if2name=ec0
```

Type:

```
:wq
init5
```

When the O2 is shut down swap also the connections, first connection between `spect` and motherboard and the second between the general net and the additional interface and reboot the O2 and than the `spect`.

2. Specifications

2. 1. Former AQX CCU Versions

The AQX_CCU is a CPU board specially designed for use in the AQX–Rack.
CCU version CU09 is the follower of CU08 with additional features. It is based on the same processor R4600 or R4700, the same IO–Subsystem but provides a modified memory interconnection and an Fast Ethernet–Subsystem. The processor–to–memory data path runs at 50 MHz and is 64 bit wide. the memory–to–IO data path is 32 bit wide and runs at 25 MHz.

AQX CCU Versions	Part No.	Layout No.	EC Level	Software Constrains	
				AspectStation	SGI Computers
CU05	H2570	H3P2050A/B/C	EC $\leq$ 19	Boot Tape 940501	all releases
CU06	H2570	H3P2050D	EC $\geq$ 20	or later	all releases
CU07	H5830 to 12/95	H3P2140	(EC00)		
CU08	H2579	H3P2130A	EC $\geq$ 0	need Unix for R4600 avail. on	
	H2570	H3P2130A	EC $\geq$ 30	Boot Tape 950901 or later	
CU08	H2570	H3P2130A	EC $\geq$ 40	need Unix for R4700 avail on diskless tree 960201 or later	
CU09 24 Prototypes	H5832 up to 7/97	H3P2160C		need Unix for R4700 avail on diskless tree 970501 or later	
CU09	H2570	H3P2160D	EC $\geq$ 50		

Table 1: AQX CCU versions

2. 2. Former AQS CCU Versions

The AQS_CCU is a CPU board specially designed for use in the new AQS–Rack.
CCU version CU10 is based on the CU09 hardware and have the same features but with the addition it contains a new extended AQS Bus System. Therefor, can be not used in the old AQX System Rack.

AQS CCU Versions	Part No.	Layout No.	EC Level	Software Constrains	
				AspectStation	SGI Computers
CU10	H9503 up to 7/98	H3P2380	EC $\geq$ 00	need Unix for R4700 avail on diskless tree 970501 or later	

Table 2: AQS CCU versions

2. 3. Features

- Operation frequency 50/25 MHz on board, 100 MHz on chip

- processor peak performance is 55 VAX MIPS (related on drystones)
- data and instruction cache size 16kbyte each
- 2 mbyte firmware
- 2 mbyte Flash EPROM Am29F016 (2,097,152 x 8–Bit)
- VME bus master interface and slave interface to the dynamic RAM
- Thin wire ethernet using Am7990
- Fast Ethernet subsystem, based on DEC 21140A, National's DP83840 and DP83223 supporting 10BaseT and 100BaseTX, Half– and Full Duplex and Autonegotiation; (100BaseT4 is not supported)
- 16–,32–,64–Mbyte dynamic RAM
- 8 RS232 channels using Z85C230, labeled as "console"or "tty00", and "tty01,...,tty09";
  2 RS485 channels using Z85C230, labeled as "tty10" and "tty20" (connectable through one 8–pin Mini–D ("console") and two 50–pin connectors ("tty01,...,tty09") at the front edge)
- real time clock MK48T02 with 2 kbyte non volatile memory
- configuration register, status register, interrupt register
- component identification channel to handle the AQX/AQS component identification system (CIS)
- JTAG Boundary–Scan controller brings the JTAG test bus to the Backplane.
- CAN Bus controller based on PCF82C200 (not implemented)

2. 4. Construction

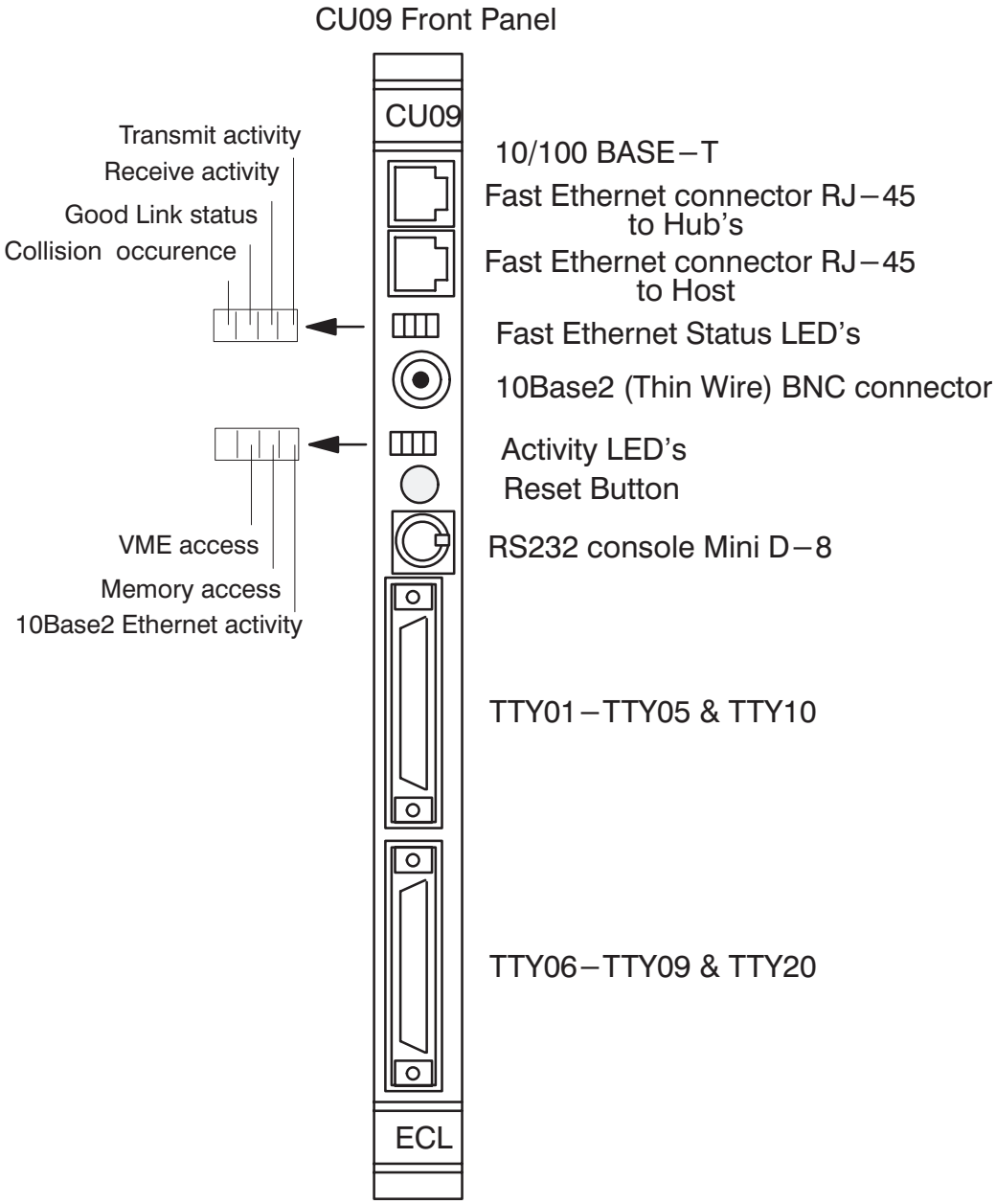
The CCU is a VME Bus module of 4 TE with an extended length. It consists of one printed circuit board.

Board Size

The real size is 233.35 mm by 280 mm . This is the so called "Double European Standard" format with a nominal plug in depth of 280 mm.

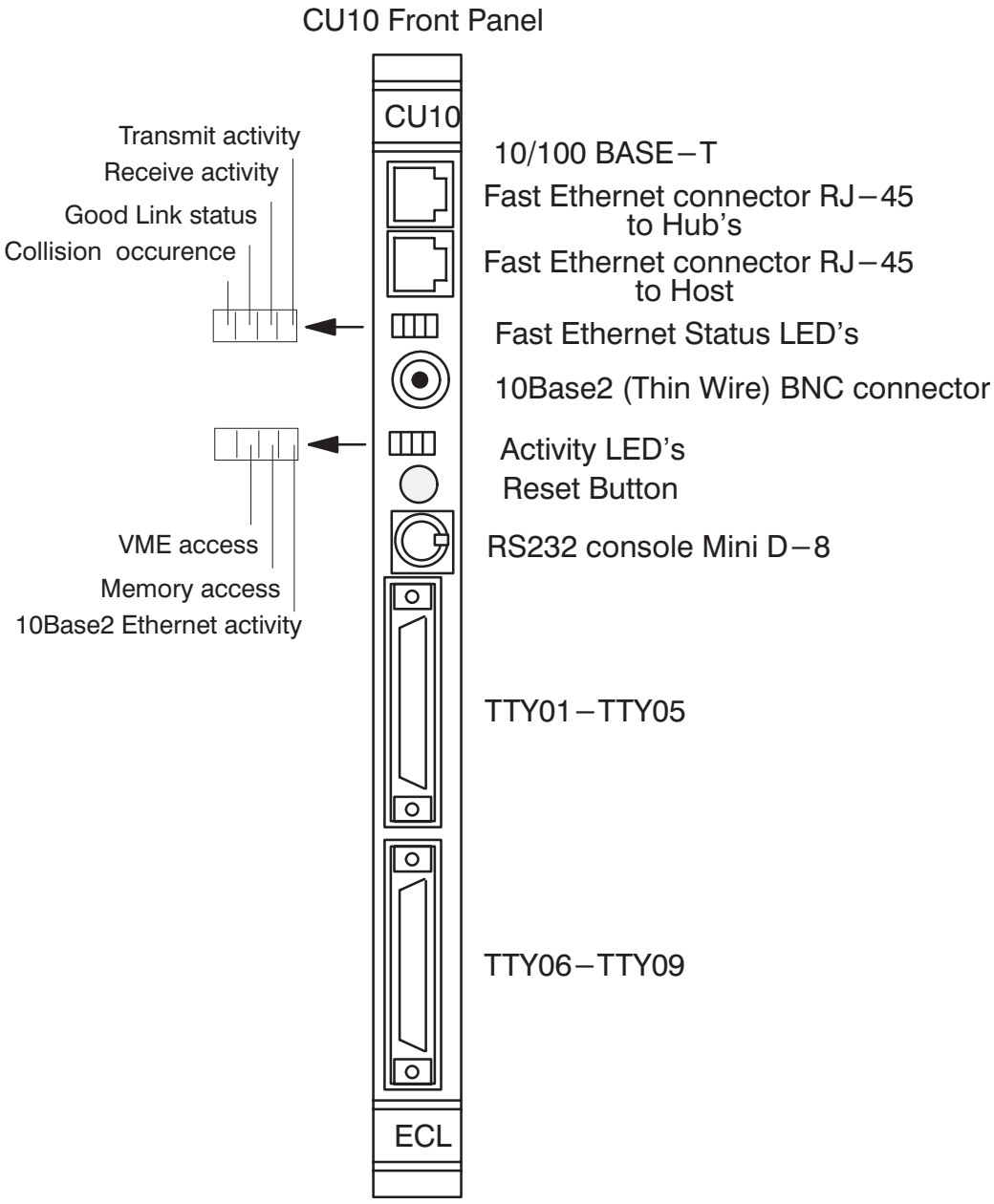
CU09 Front View

Figure 1: CU09 Controls at Front Panel



CU10 Front View

Figure 2: CU10 Controls at Front Panel



Note: TTY10 and TTY20 are available on the AQS backplane X3 connector.

2. 5. Part numbers of AQX CU09 P/N H2570

Table 3: Table of CU09 Assembly Groups

Title	Function	Part−Nr.
AQX_CCU	Assembled PCB	H5832
PCB Layout H3P2160	Plain PCB	H5833

Title	Function	Part–Nr.
CU09 PAL set		H5834
Front–Panel Assembly Set		Hz0548
Front–Panel–Ident	”CCU/9”	Hz3954

2. 6. Part numbers of AQS CU10 P/N H9503

Table 4: Table of CU10 Assembly Groups

Title	Function	Part–Nr.
AQS_CCU	Assembled PCB	H9503
PCB Layout H3P2380	Plain PCB	H9504
CU10 PAL set		H9505
Front–Panel Assembly Set		Hz06237
Front–Panel–Ident	”CCU/10”	Hz

2. 7. Accessories for CU09/10

Table 5: Part# of Accessories

Part	Part Nr.
CU09 to Terminal Cable DIN–8/D–SUB–25 male/male 3m	HZ04112
CU09 to INDY Cable DIN–8/DIN–8 male/male 10m	HZ10091
CU09 to O2 Cable DIN–8/D–SUB–9 male/female 10m	HZ04161
CU09 SCSI Cable 50p	73104
CU09 Fast Ethernet UTP CAT5 RJ45 Cable 2m	83024
CU09 Fast Ethernet UTP CAT5 RJ45 Cable 5m	83025
CU09 Fast Ethernet UTP CAT5 RJ45 Cable 10m	83026
CU09 Fast Ethernet UTP CAT5 RJ45 Cable 0,5m	67980
CU09 Fast Ethernet UTP CAT5 RJ45 Cable 3m	67981
CU09 Fast Ethernet UTP CAT5 RJ45 Cable 7,5m	67986
Cheapernet set 2*50 Ohm + 2*T–coax–connector + 10m coax	HZ03817
Cheapernet set 2*50 Ohm + 2*T–coax–connector + 25m coax	H2606
Aspect Station RS232 Router	H5468
AQX RS232/485 Extension Unit	H5714
5 Port Ethernet 10 MHz Mini Hub	O001114
AUI/10BASE–2 Micro Transceiver	
AUI/10BASE–T Micro Transceiver	O00744
8MB PS2 Modul 2MB*36 , 70ns	65173
16MB PS2 Modul 4MB*36 , 70ns	66123
32MB PS2 Modul 8MB*36 , 70ns	66124
8MB PS2 Modul 2MB*32 , 60ns	67924
16MB PS2 Modul 4MB*32 , 60ns	67946
32MB PS2 Modul 8MB*32 , 60ns	67945

Connecting to RS232/RS485 of CU09

There are two devices which can be used to adapt ”tty01,...tty09, tty10 and tty20” to the separate Sub–D–9 Connectors (see Figure 3:):

- AspectStation1 RS232 Router, (only for RS232), P/N H5468
- AQX RS232/485 Extension Unit, P/N H5714

Both devices have to be connected to the CCU by one or two cables of the following type:

- SCSI Cable P/N 73104

Connecting to RS232/RS485 of CU10

The RS485 Channels (tty10 and tty20) are only avalable at the AQS Backplane, Connector X3.

Connecting the RS232 Channels ”tty01,...tty09” to the separate Sub–D–9 Connectors the following parts can be used (see Figure 4:)

- AspectStation1 RS232 Router, (for RS232 only), P/N H5468
- AQS RS232 Extension Unit, P/N H9508

RS232 devices have to be connected to the CCU by one or two cables of the following type:

- SCSI Cable P/N 73104

Figure 3: CU09 Attaching SubD connectors to the RS232/485 interfaces

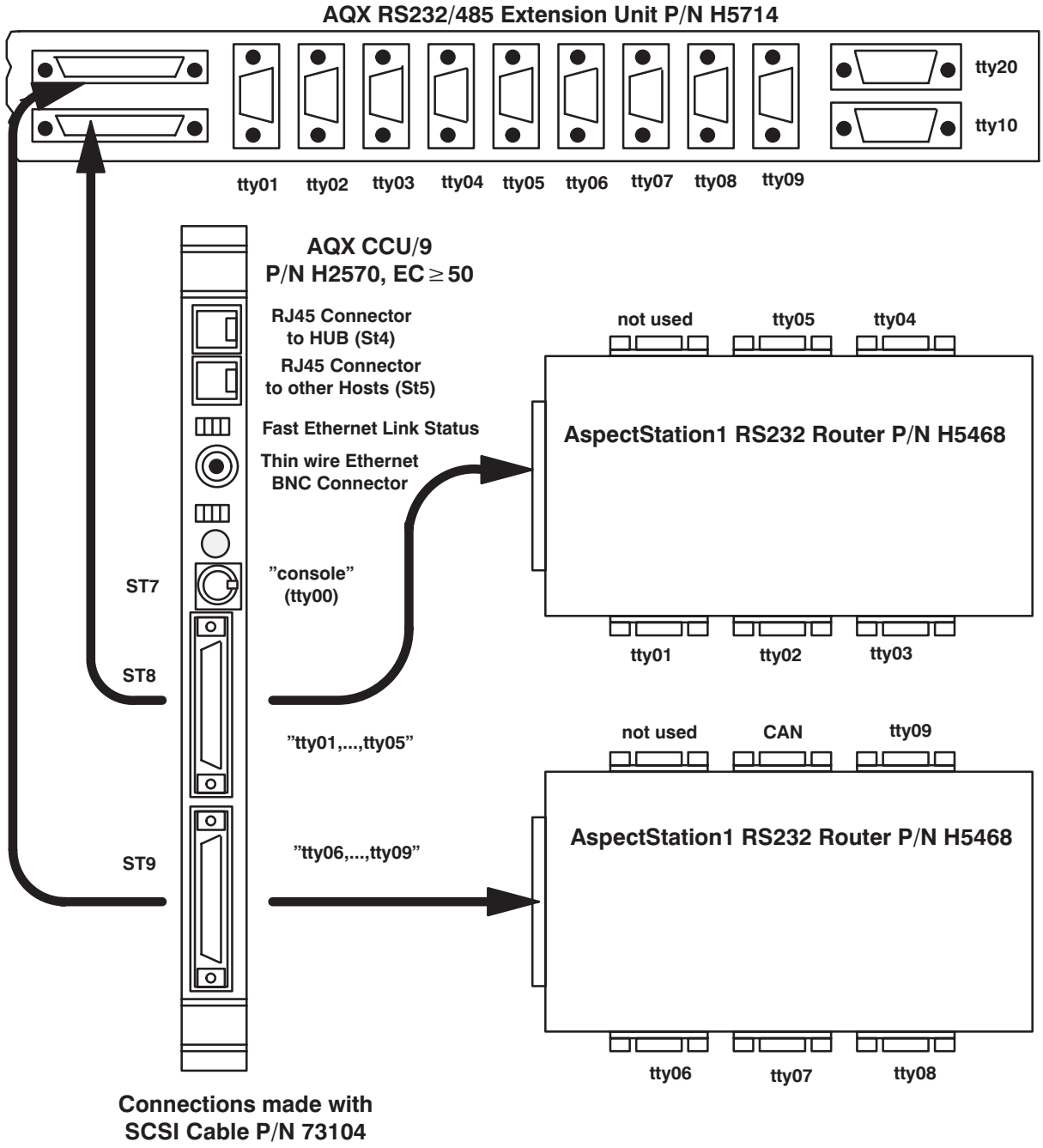


Table 6: CU09 Configuration of Serial Interfaces

UNIX Special File	/dev/tty00	/dev/tty01,...,05	/dev/tty06,...,09	/dev/tty10	/dev/tty20	/dev/can
Function	(Console)	RS232		RS485		CAN Bus
CCU Connector	ST6	ST7	ST8	ST7	ST8	ST8
AQX Ext. U. Connector	N/A	ST2,...,ST6	ST7,...,ST10	ST13	ST11	N/A

Figure 4: CU 10 Attaching SubD connectors to the RS232 interfaces

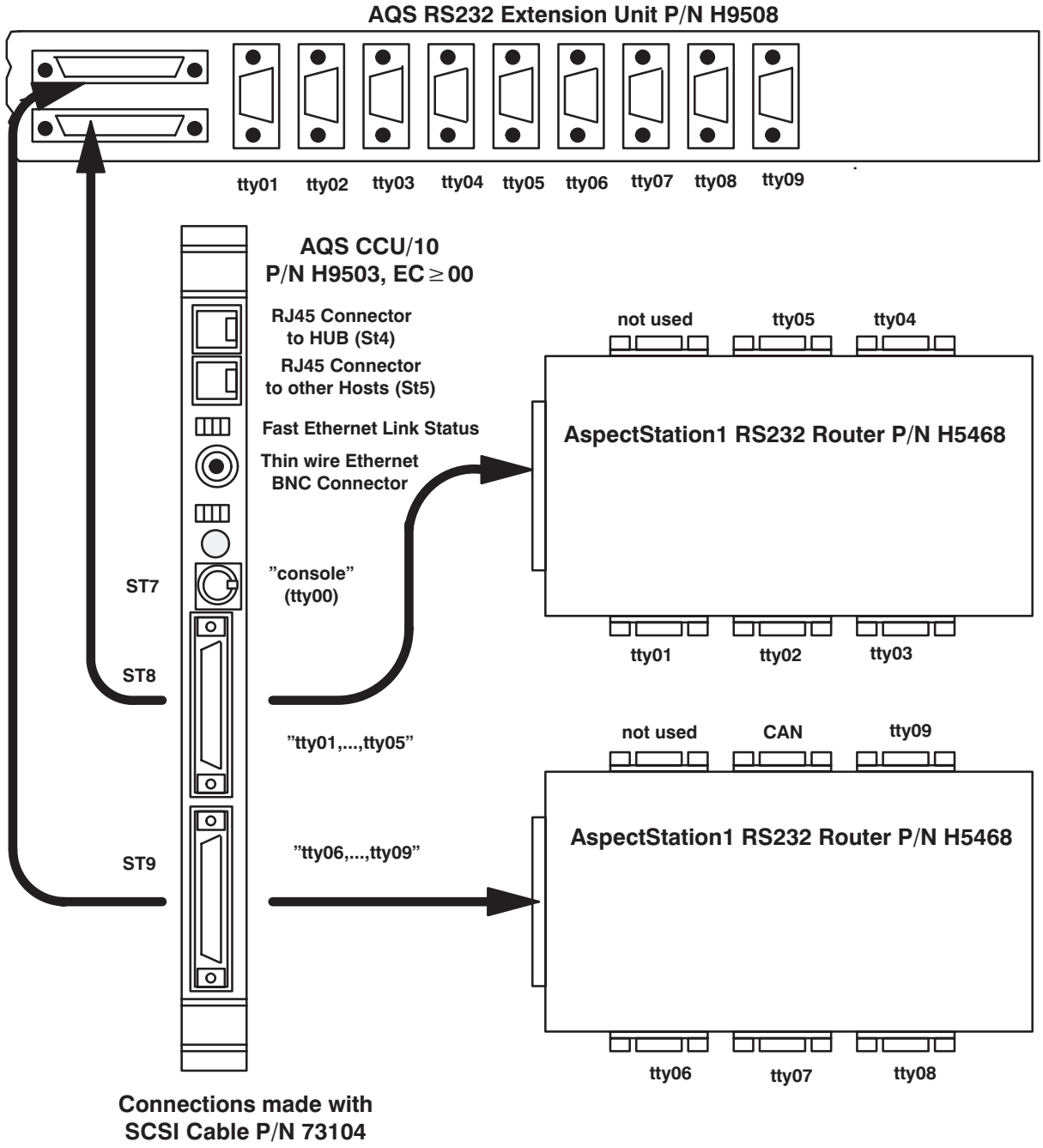


Table 7: CU10 Configuration of Serial Interfaces

UNIX Special File	/dev/tty00	/dev/tty01,...,05	/dev/tty06,...,09	/dev/tty10	/dev/tty20	/dev/can
Function	(Console)	RS232		RS485		CAN Bus
CCU Connector	ST6	ST7	ST8	ST2	ST2	ST8
AQS Ext. U. Connector	N/A	ST2,...,ST6	ST7,...,ST10	N/A	N/A	N/A

Connecting to the Console

- CU09/O2 console cable 10m P/N HZ04161

This is the CU08/Indy console cable which can be used for CU09 in reverse direction.

- CU09/Terminal console cable 3m P/N HZ04112

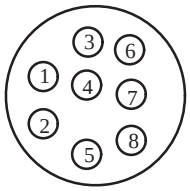
This cable was originally designed to connect a plotter to the Indy.

Figure 5: Console Cable, MINI D, 8 pin to D_SUB, 9 pin

Pin #	Signal
1	DTR
2	CTS
3	TxD
4	GND
5	RxD
6	RTS
7	DSR
8	GND

MINI D, 8 pin, male

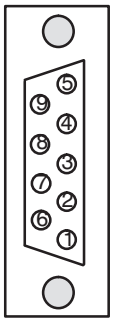
Plug, front view



Pin #	Signal
1	Shield
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	NC

D−sub. 9pin, female

Plug, front view



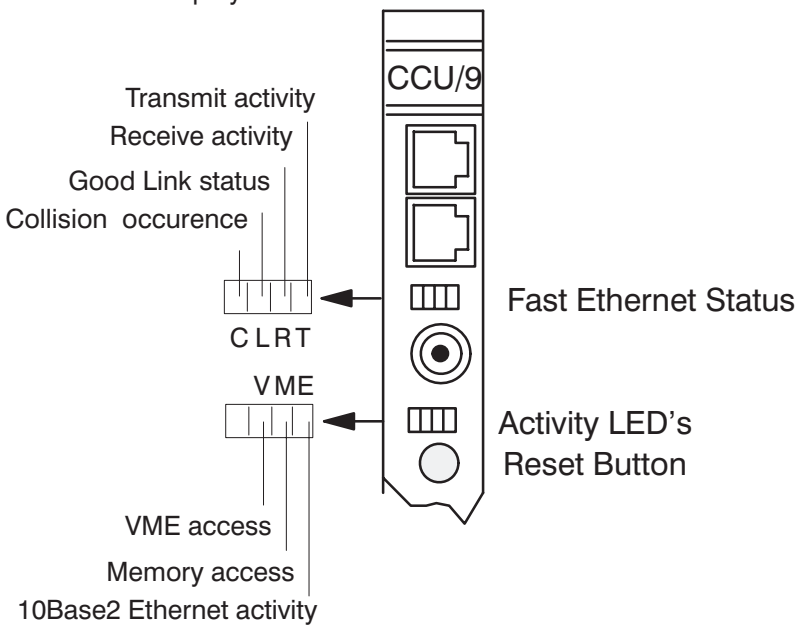
Connecting to Fast Ethernet

- 10–MBit Mini Hub, Part# O001114
- Fast Ethernet Cable Types

Cable Type	Category	Part Number	Length
UTP	CAT 5	83025	5m
UTP	CAT 5	83026	10m

2. 8. Controls and Indicators

Figure 6: Front View at LED Display and Reset Button



Reset Button

- The general hardware reset signal of CCU and VME–Bus can be initiated by pushing the ”Reset Button”. It stays active for about 80 milliseconds.

Activity LED's

The 4 digit LED–Display forms a hexadecimal coded value with MSB at the left side. Lighting reflects a logical ”One”.
The display shows the 4 bit contents of the Status–Register (see Figure 6:) written on D7–D4 if this value is less than 8, usually after power–up or reset.
If the MSB is set in the Status–Register the lower 3 digits from right to left reflect the activities of the Ethernet–DMA, the CPU access to DRAM and the activity of the CPU on VME bus.

The intention is that after power–up or reset a basic test procedure changes the LED value at success in steps from zero up to eight where eight means all tests have been passed and the monitor is running.

Fast Ethernet Status LED's

The status information is available on the LED outputs pins of the DP83840.

LED1	Transmit activity, DP83840 pin 42
LED2	Receive activity, DP83840 pin 41
LED3	Good Link Status, DP83840 pin 38
LED4	Collision, DP83840 pin 36
”Collision ”	ON indicates the occurrence of collisions in 10BASE–T or 100BASE–TX operation.
”Good Link Status”	ON indicates valid link on the network connection and ready state for normal operation.

	OFF indicates that the PHY did not find a valid link on the network connection. Transmit and receive operation are not possible. In this situation the hardware is performing Autonegotiation without any software interaction.
”Receive Activity”	ON indicates that a packet is being received in 10BASE–T or 100BASE–TX mode.
”Transmit Activity”	ON indicates that a packet is being transmitted in 10BASE–T or 100BASE–TX mode.

2. 9. Operational Settings

2. 9. 1. NVRAM Setting

The NVRAM contains a set of parameters which are used by the software. After power up, the monitor checks the parameter called `magic`.. If `magic`. is anything else than `RISCPROM`, e.g. if a new and empty NVRAM has just been inserted, the monitor does the whole set of diagnostic tests and sets the NVRAM parameters to the following default values:

```
netaddr=0x149.236.99.99
netmask=0xffffff00
lbaut=9600
rbaut=9600
bootfile=bfs()/usr/diskless/clients/spect/root/unix
bootmode=c
console=0
cpuid=0
resetpc=xxxxxxxx
resetra=xxxxxxxx
eth_addr_ch1=0x
eth_addr_ch2=0x
version=5.40
magic=RISCPROM
model=CCU R4600
vendor=BRUKER
rootname=0
use_bootparams=1
keyswtch=0
keyboard=AT
```

This procedure takes a few minutes. The monitor prints a test protocol and at last its prompt (>>) on `tty0` which is the default `console output`.

The NVRAM parameters can be printed with the monitor by

`printenv`

and can be changed by

`setenv` *`parameter value`*

A problem crops up if `magic` is equal to `RISCPROM` and `lbaud` and `rbaud` doesn’t meet the bauderate of the connected terminal or `console` doesn’t meet the interface to which the terminal is connected to. Then no printout or input is possible. To correct this

NVRAM, you have only the chance to insert it into a running CCU without powering off and set the parameters to their correct values or clear `magic` to an other value than `RISCPROM`.

Table 8: Parameters to be set

Parameter	Recommended value	Values	Declaration
console	0	0	The monitor uses tty0 as console. This is the default value if `magic` 0 `RISCPROM` and the monitor initializes the NVRAM
		L	The monitor tries to use the graphic channel as console or tries using `tty0` or `tty1`, if the graphic channel can't be opened.
		C	Only the graphic channel will be used.
bootmode	c	m	The monitor runs all the diagnostic tests after power up and sets boot mode to "c"
		c	The monitor clears the memory after reset and boots without doing any test.
		d	The boot procedure has to be started by typing `u` or `auto` the memory will not be cleared and no tests will be carried out.
eth_addr_ch1			Physical ethernet address of the Thin Wire (10Base2) interface
eth_addr_ch2			Physical ethernet address of the Fast Ethernet (10/100BaseT) interface
boot_params	1	0	The monitor tries to boot from a hard disk and a file named by `bootfile`
		1	The monitor booted the bootfile over the net by means of the bfs–deamon.
bootfile			Path and file to be booted

2. 9. 2. Configuration

Some features or properties of CU09/10 were adjusted in the factory or may be later configured.

Firmware version

- The originally installed and labeled firmware Prom's are "2–jjmmdd" containing the two high bytes and "1–jjmmdd" containing the low bytes.

Installed type of firmware Prom's

- A choice out of 2 types is possible, 2 devices in PLCC–Package are required.
- W11 removed: 272048 may be used resulting in 512 kbyte
- W11 inserted: 274096 can be used resulting in 1 megabyte firmware space
- Access time is required to be 120 nsec or less

SYSCLK on VME Bus

- Jumper W10 connects if inserted the cpu clock to SYSCLK of the VME Bus.

Ethernet/Cheapernet Configuration

- Jumper W2 inserted in position B makes the cheapernet to send a SQE test sequence, W2 in position A disables the SQE test mode, e.g. if there is a Repeater connected.

2. 9. 3. Installing DRAM

- It is possible to equip the CCU with 16, 32 or 64 Mbyte using 2 of
  8–Mbyte DRAM modules (P/N 65173),
  16–Mbyte DRAM modules (P/N 66123) or
  32–Mbyte DRAM modules (P/N 66124).
  The modules have to be inserted as U75 and U76.
  Furthermore this needs W7 to be set and the following jumper setting of W5 position A and B :

Inserted Jumper in position A and B of W5	Corresponding logic signals SEL0, SEL1	CU09/10	
		DRAM Size	Module Equipment
A,B	0,0	16 Mbyte	2 x 8 Mbyte as U75,U76
A,–	0,1	32 Mbyte	2 x 16 Mbyte as U75,U76
–,–	11	64 Mbyte	2 x 32 Mbyte as U75,U76

Table 9: DRAM configuration

- Any installed DRAM is not available if W7 is removed

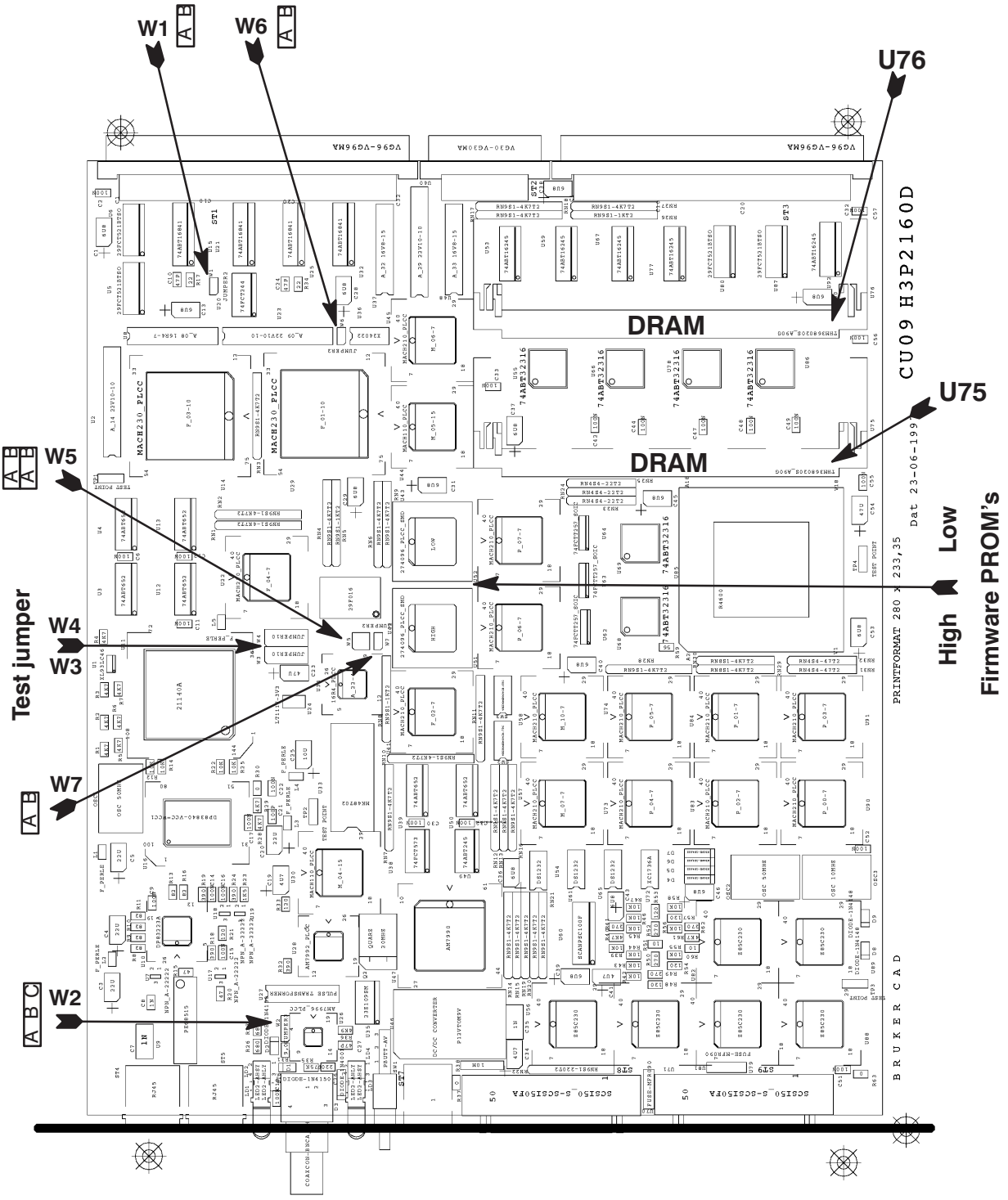


Figure 7: Jumper, Prom and DRAM Locations for CU09

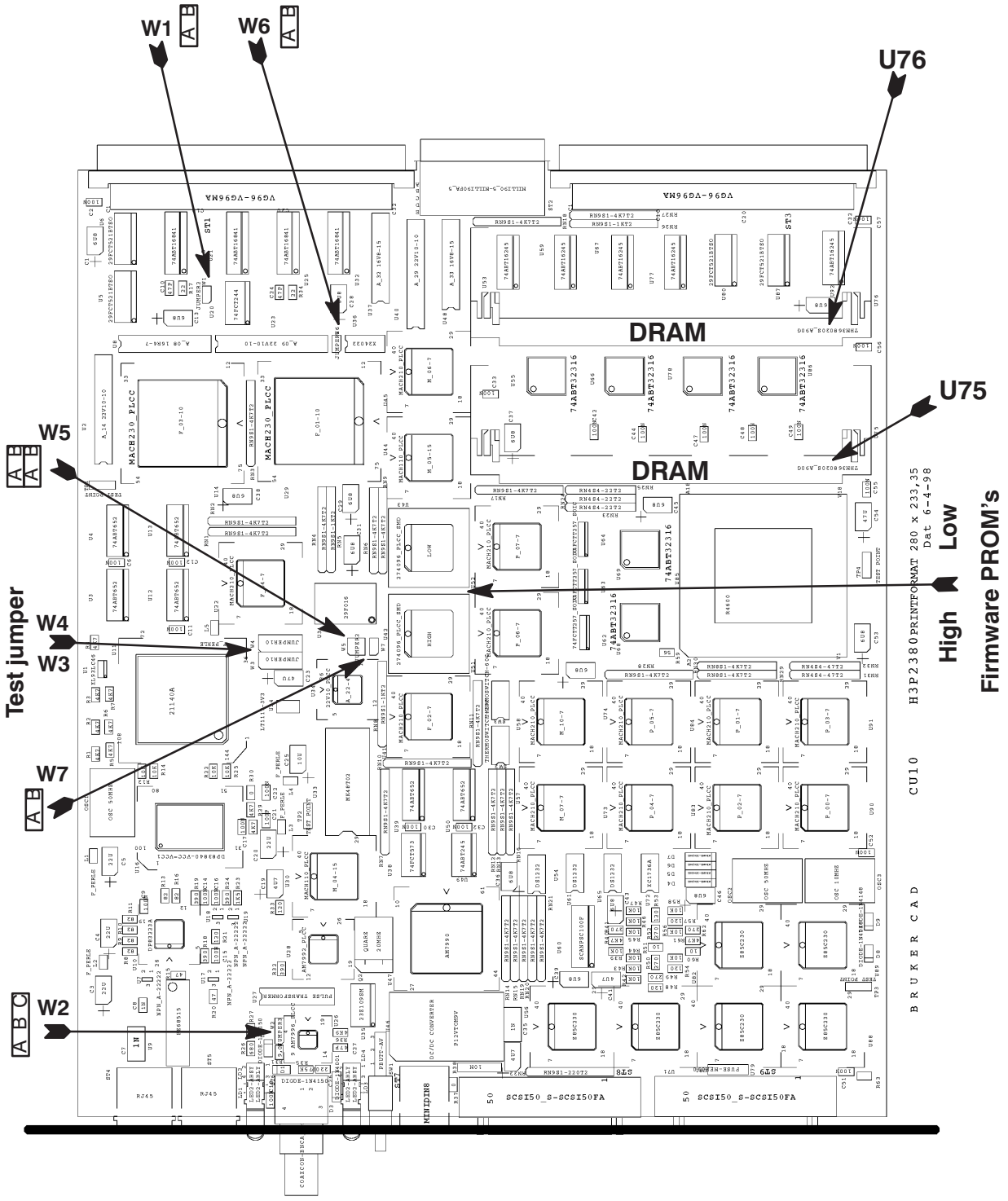


Figure 8: Jumper, Prom and DRAM Locations for CU10

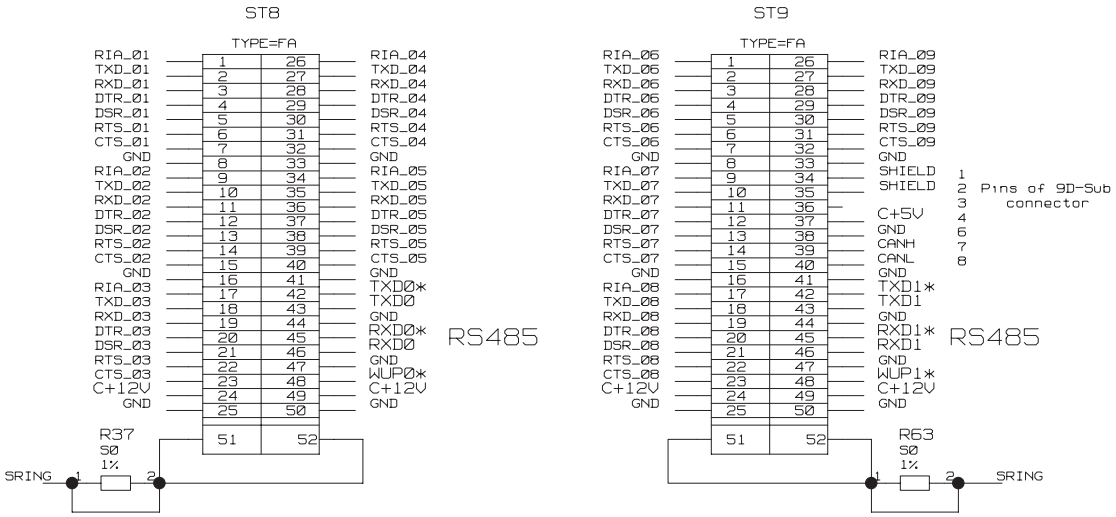
2. 10. Connectors and Signal Allocations

Table 10: RS232 Signal assignments

Devices	CU09/10	INDY	O2	Terminal
Connectors	Mini DIN–8	Mini DIN–8	D–SUB–9	D–SUB–25
Signal	**Pin#**			
Shield	housing	housing	housing	1
DTR	1			5
CTS	2	6	7	20
TxD	3	5	2	3
GND	4	4	5	7
RxD	5	3	3	2
RTS	6	2	8	6
DCD	7			4
GND	8			

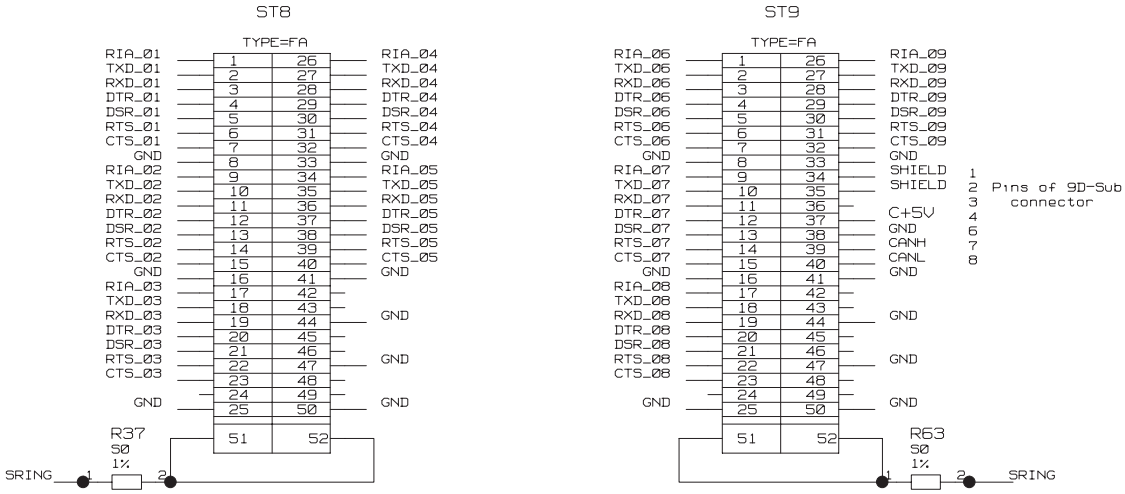
CU09 ST8/ST9 ”tty01,...,tty09,tty10,tty20” RS232–Connector

Figure 9: AMP Amplimite 050, 50 pin, female



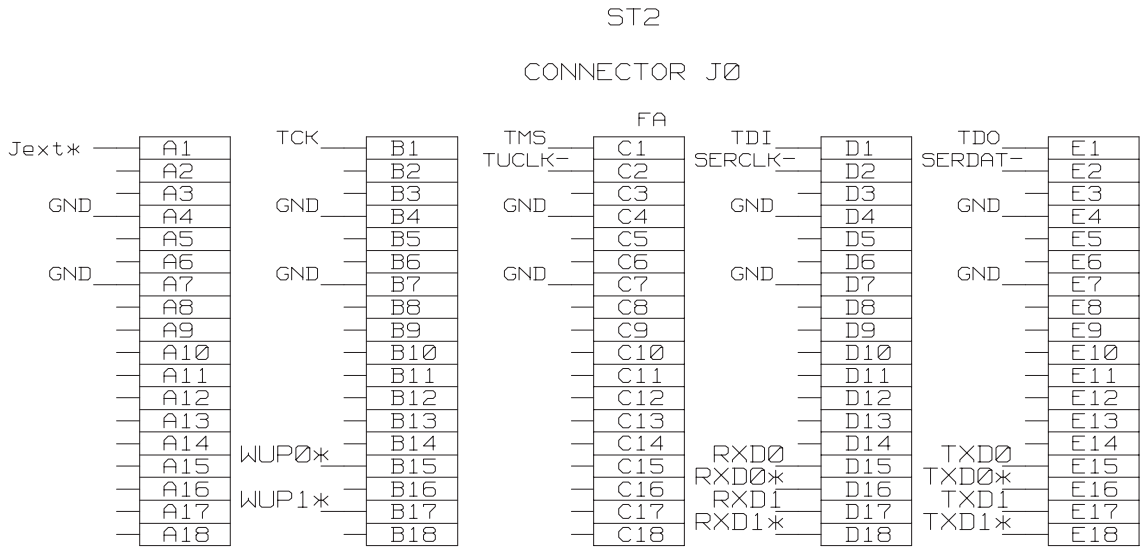
CU10 ST8/ST9 ”tty01,...,tty09,” RS232–Connector

Figure 10: AMP Amplimite 050, 50 pin, female



CU10 ST2 ”tty10,tty20,” RS485, JTAG and BBIS–Connector

Figure 11: Mini Metral 90 pin, female

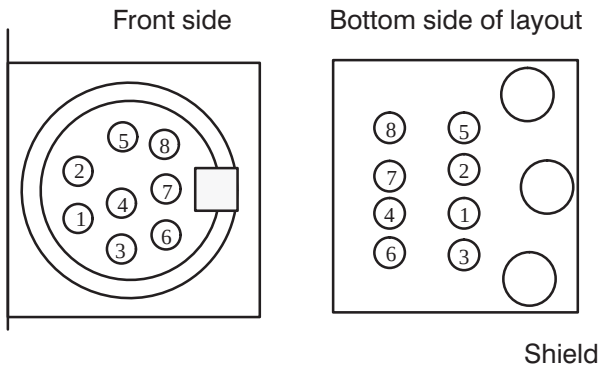


RS485 Interface
TTY10, TTY20

ST7 ”Console” (tty00) RS232–Connector

Figure 12: Console Connector at CCU, MINI D, 8 pin, female

Pin #	Signal
1	DTR
2	CTS
3	TxD
4	GND
5	RxD
6	RTS
7	DSR
8	GND



Fast Ethernet signal assignment at the RJ45–8 connectors

The twisted pair Ethernet requires a category 5 (CAT5) unshielded twisted–pair (UTP), 2–pair cable for a 100BASE–TX network connection or a category 3 (CAT3), or higher UTP cable for a 10BASE–T network connection.

The standard twisted–pair cable has a straight–through pin to pin connection from plug to plug.
The star topology of twisted pair Ethernet connecting several Hosts via one Hub requires a different signal assignment between Hub and Host side.
The CU09/10 provides both assignments at 2 RJ45 sockets which enable it to be connected to other Hosts via an Hub (standard way) or without an Hub (point–to point).

Figure 13: RJ45 Pin numbering

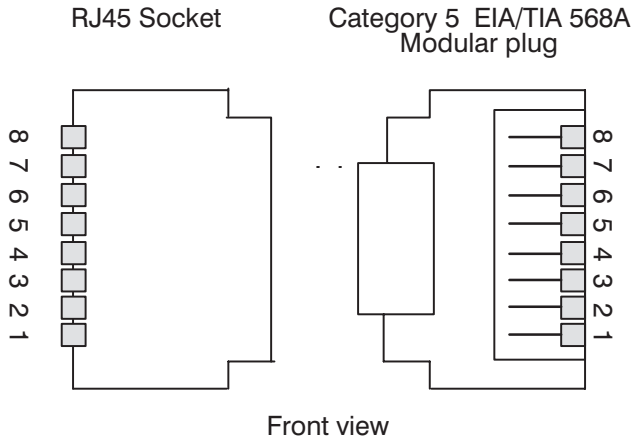


Figure 14: Fast Ethernet Signal Assignment

Pin #	Cable Color Codes	Connector ”FETH to Hub”	Connector ”FETH to Host”
1	White–Orange	TX+	RX+
2	Orange	TX–	RX–
3	White–Green	RX+	TX+
4	Blue	NC	NC

5	White−Blue	NC	NC
6	Green	RX−	TX−
7	White−Brown	NC	NC
8	Brown	NC	NC

2. 11. Power Requirements

The CU09 requires power supply of the following voltages:

	Part− No.	+5 V	+12 V	−12 V	+5 V analog J3: C8	−5 V analog J3: C1,...,C5
CCU: CU09/10	H2570 / H9503	5,3 A	0,3 A	0,1 A	0	0

CU09 supplies fused current at the following connectors:

ST8/9 RS485 +12 Volt 0.2 Ampere

The resistance of the fuse will be suddenly growing with temperature caused by high current. The fuse recovers when cooling down and need not be replaced.

3. Service Information

3. 1. Operating Conditions

(see also Chapter 1.)

Modifications

No device already be used with CU08 in AQX system needs any modification.

The CU10 can be used in AQS system only.

Software

CU09/10 with Fast Ethernet needs the `unix 970501` included in `xwin–nmr2.0` or later.

The Thin Wire Ethernet (10Base2 or so called Cheapernet) is still available but can not be run by the ”unix 970501” included in ”xwin–nmr2.0”. A later version will manage both ethernet devices.

AQX Assembling

CU09 has to be inserted in the same slot as CU08.

All connections can be carried out as on CU08. The BNC cable of the Thin Wire Ethernet (10Base2) should be left unconnected. 10Base2 is considered to be obsolete on CU09 and no longer available.

AQS Assembling

CU10 has to be inserted in the first slot of AQS rack.

All connections can be carried out as on CU09 with the exception of the RS485 interface that is now available on the AQS backplane. The BNC cable of the Thin Wire Ethernet (10Base2) should be left unconnected. 10Base2 is considered to be obsolete on CU10 and no longer available.

3. 2. Network connection

The Fast Ethernet of CU09/10 is to be connected to the first or second ethernet interface on O2, the so called `ec0` or `ec1` (see workaround).
There are two RJ45 Fast Ethernet sockets on CU09/10. They are connected inside to the same signals but have crossed pin assignments.
The upper socket (signed ”FETH–HUB”) has to be used if CU09/10 will be connected to an HUB. This is the normal way with twisted pair ethernet hosts.
The lower socket (signed ”FETH HOST”) has to be used to connect CU09/10 by the same normal cable to another host (point–to–point connection).
That means, connect CU09/10 from socket ”FETH HOST” to the Host by one of the following accessories:

Connection Kits

To O2

Part	Part Number	Length
Fast Ethernet Cable UTP Cat5	83025	5m
	83026	10m

Console Cable to Terminal	HZ04112	
Console Cable to O2	HZ04161	

To Indy

Part	Part Number	Length
Fast Ethernet Cable UTP Cat5	83025	5m
	83026	10m
Console Cable to Terminal	HZ04112	
Console Cable to Indy	HZ10091	
10BaseT Micro transceiver	O00744	

The Fast Ethernet will adjust itself to the 10 MHz speed of the Indy.

To Aspectstation

Part	Part Number	Length
Fast Ethernet Cable UTP Cat5	83025	5m
	83026	10m
Console Cable to Terminal	HZ04112	
Console Cable to Aspectstation	HZ04161	
10BaseT Mini Hub	O001114	

The LINK Led (2. led from left in upper row) shows a good link status after power up. Otherwise one of the two link partners is down by software or power. The Fast Ethernet cable can be pulled out and plugged in under power and activity. Autonegotiation and link checking starts on both partners without software interaction if the link has been broken.
Unplugging, powering down or typing **`ifconfig ec1 down`** on O2 or **`ifconfig fen down`** on `spect` break the link.

3. 3. Software Implementation

Fast Ethernet needs the `unix 970501` included in `xwin-nmr2.0` or later.

The ethernet address of the exchanged CU08 has to be cleared on the Host by typing

`/etc/arp -d spect` on Aspectstation and
`/usr/etc/arp -d spect` on Indy and O2

Suggestion

If you, nevertheless, meet problems in booting the `spect` and before you try it again, you should expect the O2 (`ec0` or `ec1`) to be in an undefined state and type:

```
ifconfig ecx down
ifconfig ecx up
```

depending on the interface to which the `spect` is connected to.

3. 4. Problems of Point–to–Point Connection to the O2

Both link partners of a Fast Ethernet Connection exchange their abilities (10 or 100 MBit and Half or Full Duplex) after power up and without software interaction. They decide then for the fastest common possibility. This procedure is called Autonegotiation respectively Parallel Detection.

The main interface of the O2 is only able to operate in Half Duplex like an Hub. The secondary interface is ready for Full Duplex but there is no software support for this on O2. The CU09 is able to run Half and Full Duplex.

This situation leads to an improper mode decision and to a Full Duplex link at the secondary interface which can't work.
To ensure an Half Duplex decision, the Full Duplex mode is switched off on CU09/10 by software (Prom version 97/06/11 and Unix version 97/05/01 in `xwin–nmr2.0`). This decreases the performance by at least 10 % and leads to collisions.

Furthermore, the point–to–point connection with O2 causes errors during the boot sequence.
This problem can be solved by connecting the O2 to the CU09/10 via an Hub or by connecting the CU09 to the main interface of the O2 (which behaves like an Hub).

Workaround

Swap logically both ethernet devices of the O2. That means, connect the `spect` to ethernet controller `ec0` on the motherboard of the O2. This can easy be carried out by modifying the file `netif.options`.

Type on O2 as superuser:

```
vi /etc/config/netif.options
```

This file contains the 2 parameter entries of `if1name=ec0` and `if2name=ec1`. Swap the values of both parameters to:

```
if1name=ec1
if2name=ec0
```

Type:

```
:wq
init5
```

When the O2 is shut down swap also the connections, first connection between `spect` and motherboard and the second between the general net and the additional interface and reboot the O2 and than the `spect`.

3. 5. Handling

3. 5. 1. Ifconfig down/up Procedure

A network subsystem can be made passive by `ifconfig down` and re–initialized by `ifconfig up`. These commands trigger off the following actions:

Ifconfig down

- Stops Receive and Transmit State Machines of the MAC (Media Access Controller)
- Clears up the descriptor list
- Resets PHY (Physical Layer) and MAC
- Starts Autonegotiation

Ifconfig up

- Executes startup procedure and initializes MAC and PHY
- Configures the descriptor list
- Waits for and interprets the Autonegotiation results
- Sets network operation mode

`ifconfig down` and `ifconfig up` are useful to clear up dubious states of the network interface. Type on `spect`:

```
ifconfig name down
ifconfig name up
```

The logical names of the network subsystems on CU09/10 are:

`fe0`	Fast Ethernet, 10/100 BaseT
`la0`	Thin Wire Ethernet, 10 Base2 (if available)

3. 5. 2. Switching the boot interface

CU09/10 can boot over Fast Ethernet or Thin Wire Ethernet 10Base2 (if available). The controller to be used can be determined by its logical name between the brackets of the `bfs`–call included in the CU09/10 boot command:

```
boot -f bfs(0,la)/usr/diskless/clients/spect/root/unix
```

This call leads to booting over 10Base2. The CU09/10 monitor will boot over Fast Ethernet if **`fe`** is inserted instead of **`la`** or as default if no name is set:

```
boot -f bfs()/usr/diskless/clients/spect/root/unix
```

If the boot procedure is called by the monitor commands `u` or `auto` the parameter of the `bootfile` in NVRAM will be used.
This parameter can be set in the monitor like this:

```
setenv bootfile bfs(0,la)/usr/diskless/clients/spect/root/unix
```

The boot procedure can be interrupted by typing **`Ctrl C`**.

3. 6. Ethernet addresses

The Ethernet address consists of 12 hexadecimal digits. The 6 leftmost ones are the constant Bruker Code, the 2 rightmost ones identify a special group of Bruker devices. The rest of them build the consecutively numbered ethernet address of each device.

To the 2 Ethernet subsystems of CU09/10 will be assigned addresses out of group 09 (Fast Ethernet) and out of group 06 (10Base2).

10Base2 Ethernet (la) on AQX CCU/9 with R4700	Status	Date	Serial# /Name	Ethernet Address		
				Bruker OUI	Device	Group
Prototypes	begin		2000	**0000ad**	0300	**06**
Series Production	begin					**06**

Fast Ethernet (fe) on AQX CCU/9 with R4700	Status	Date	Serial# /Name	Ethernet Address		
				Bruker OUI	Device	Group
Prototypes	none		2000	0000ad	0000	09
Series Production	begin					09

10Base2 Ethernet (la) on AQS CCU/10 with R4700	Status	Date	Serial# /Name	Ethernet Address		
				Bruker OUI	Device	Group
Series Production	begin		0010	0000ad	0000	06

Fast Ethernet (fe) on AQS CCU/10 with R4700	Status	Date	Serial# /Name	Ethernet Address		
				Bruker OUI	Device	Group
Series Production	begin		0010	0000ad	0000	09

3. 7. Introduction Status of the AQX CU09 CCU

3. 7. 1. Modifications of the introduced layout

There are 25 prototypes of CU09 using layout H3P2160C with some modifications.
The PCB layout put into production is H3P2160D without any modification.

3. 7. 2. Jumper Configuration

Normal setting of installed jumpers:

W4	A+B (16 Mbyte DRAM with 2 8Mbyte SIMM's)
W1	not set
W12	C
W6	not set
W10	set
W11	not set
W3	set
W2	set in pos. B
W7	set in pos. B and C
W8, W9	nothing to set, test signals

3. 7. 3. Configurations of the introduced layout

CCU configuration of Serial Interfaces:

	CU09						
UNIX Special File	/dev/tty00	/dev/ tty01,...,05	/dev/ tty06,...,07	/dev/tty08	/dev/tty09	/dev/tty10	/dev/tty20
Function	(Console)	RS232				RS485	
CCU Connector	ST7	ST8	ST9	ST9		ST8	ST9
AQX Ext. U. Connector	N/A	ST2,...,ST 6	ST7,...,ST 8	ST9	ST10	ST13	ST11

CCU DRAM configuration:

```
Select Jumper W6

SEL0  1 o----o 2 SHORT

SEL1  3 o    o 4 OPEN
```

SEL1, SEL0	W6	SIZE	SIMM's
00	1o----o2 3o----o4	16MB	2x8 MB P/N 65173 or P/N 67924 as U75, U76
10	1o o2 3o----o4	32MB	2x16 MB P/N 66123 or P/N67946 as U75, U76
11	1o o2 3o o4	64MB	2*32 MB P/N 66124 or P/N67945 as U75, U76

Note: Any installed DRAM module is not available if jumper W7 is removed

The new CCU version need following software

- Boot PROM version: 970611
- Diskless version: 970501 included XWIN NMR 2.0 release

3. 8. Introduction Status of the AQS CCU10

3. 8. 1. Modifications of the introduced layout

The new AQS CCU CU10 board contains the same functions as the previous CU09 P/N H2570
excepted the middle J0/ST2 connector for the backplane which has been changed . Additionally, the RS485 interface is connected to the J0/ST2 connector and now available on the backplane X3 connector. Therefore, it is physically not compatible with the old AQX system.

3. 8. 2. Jumper Configuration

Normal setting of installed jumpers:

W4	A+B (16 Mbyte DRAM with 2 8Mbyte SIMM's)
W1	not set
W12	C
W6	not set
W10	set
W11	not set

W3	set
W2	set in pos. B
W7	set in pos. B and C
W8, W9	nothing to set, test signals

3. 8. 3. Configurations of the introduced layout

CCU configuration of Serial Interfaces:

	CU10						
UNIX Special File	/dev/tty00	/dev/ tty01,...,05	/dev/ tty06,...,07	/dev/tty08	/dev/tty09	/dev/tty10	/dev/tty20
Function	(Console)	RS232				RS485	
CCU Connector	ST7	ST8	ST9	ST9		ST2	ST2
AQX Ext. U. Connector	N/A	ST2,...,ST 6	ST7,...,ST 8	ST9	ST10	N/A	N/A

Pin out of the X3 connector at the AQS backplane :

	Signal		**Signal**
2	TxD−_1	1	TxD+_1
4	GND	3	GND
6	RxD−_1	5	RxD+_1
8	SGU Stop	7	WUP_1
10	+12V	9	+12V
12	+12V	11	+12V
14		13	WUP_2
16	RxD−_2	15	RxD+_2
18	GND	17	GND
20	TxD−_2	19	TxD+_2

Note: UNIX Special Files for RS485 interfaces

/dev/tty10: TxD–/+ 1, RxD–/+ 1, WUP 1
/dev/tty20: TxD–/+ 2, RxD–/+ 2, WUP 2

CCU/10 DRAM configuration:

```
Select Jumper W5

SEL0  1 o----o 2 SHORT

SEL1  3 o    o 4 OPEN
```

SEL1, SEL0	W5	SIZE	SIMM's
00	1o----o2 3o----o4	16MB	2*8 MB P/N 65173 or P/N 67924 as U75, U76
10	1o o2 3o----o4	32MB	2*16 MB P/N 66123 or P/N67946 as U75, U76
11	1o o2 3o o4	64MB	2*32 MB P/N 66124 or P/N67945 as U75, U76

Note: Any installed DRAM module is not available if jumper W7 is removed

The new CCU version need following software

- Boot PROM version: 970611
- Diskless version: 970501 included XWIN NMR 2.0 release

3. 8. 3. 1. NVRAM

The way how you can set the NVRAM parameters to the right value depends on the value of its parameter "**magic**".

The Firmware sets after power up the NVRAM parameters to the right values and runs the Power–on–Diagnostics if it detects "magic"as not equal to "RISCPROM" assuming the NVRAM to be virgin.
Starting with Firmware Version "199990408" the Power–on–Diagnostics will be first carried out at the second boot procedure.

If magic=RISCPROM the Firmware will boot normally but if the parameters "bauderate" or "console" are incorrect, you have only the chance to insert this NVRAM without switching power off into a CPU running in monitor and set "magic" to an other value than RISCPROM.

The following parameters have to be corrected.

console

"0"	The monitor uses tty0 as console. This is the default value if magic ≠ RISCPROM and the monitor initializes the NVRAM
"L"	:the monitor tries to use the graphic channel as console or tries using tty0, tty1, if the graphic channel can't be opened
"C"	:only the graphic channel will be used

bootmode

"m"	: the monitor runs all the diagnostic tests after power up and sets boot mode to "e"
"e"	:the monitor clears the memory after reset and boots without tests

”d” :the memory will not be cleared and no tests will be carried out during boot procedure

eth_addr_ch1, eth_addr_ch2

The parameters `eth_addr_ch1` and `eth_addr_ch2` are located in the write protected range of the NVRAM. They can only be modified if the PAL device CU09Fx01 is replaced by CU09NP01 which is only available to the service staff.

Recommendet Parameter Setting

```
netaddr=0x149.236.99.99
netmask=0xffff0000
lbaut=9600
rbaut=9600
bootfile=bfs()/usr/diskless/clients/spect/root/unix
bootmode=c
console=0
cpuid=0
resetpc=xxxxxxxx
resetra=xxxxxxxx
eth_addr_ch1=0x0000ad03xx06
eth_addr_ch2=0x0000adxxxx09
version=5.40
magic=RISCPROM
model=CCU R4600
vendor=BRUKER
rootname=0
use_bootparams=1
keyswtch=0
keyboard=AT
```

3. 8. 3. 2. Firmware

CU09/10 needs the firmware version 97/05/01 or later. It is put into production with version 97/06/11. This version declares CU09/10 during autonegotiation as being able to send in half duplex mode only. This is to work around the bugs of the O2.
The monitor prints in the beginning of the boot procedure its choice

```
10 BASE-TX Half-Duplex
```
or
```
100 BASE-TX Half-Duplex
```

depending on the abilities of its link partner.

The firmware is configured as 4 byte wide and accommodated in 2 prom devices. One for the upper and lower 2 bytes each.

Table 11: Firmware Proms

Name	Label	Function	Device	Type	Part#
CU09EA01	1−97/06/11	2 high bytes	U42	M27C4002 −120C	H9133
CU09EA02	2−97/06/11	2 low bytes	U43		H9133

The firmware prom's are listed in the PAL part list.

3. 8. 3. 3. Serial Boot Prom

The processor R4700 reads some internal operational settings out of a serial boot prom at power up. The prom volume is 256 bits. The first 15 bits are valid. The rest is reserved and have to be clamped to zero.

Table 12: Boot Prom

Serial Bit	Meaning
0	Reserved and zero
1 to 4	Block write data mode and ratio
5 to 7	Clock ratio between internal and external clock
8	Endian ordering
9 to 10	Non–block write handling
11	Enable of timer interrupt
12	Reserved and zero
13 to 14	Output driving slew rate
15 to 255	Reserved and zero

The serial boot prom is listed in the PAL part list. It is named CU09EA00 and labeled "EA" or "50MHz".

3. 9. AQX CU09 CCU History of Modifications

EC No.	Date	Part Number	Description of Bugs, Changes and Modifications	Ser.No.	New EC – Level
			CU09 Prototypes, H3P2160C	2000–2020	
			CU09 Prototypes, H3P2160D	2021–2025	
2435	8.10.97	H2570	Introduction of AQX CCU CU09 Layout version H3P2160D	2301	50
2455	12.1.98	H2570	Correct Part List to the originally used Clock driver with CMOS signal level IDT49FCT805ASO20–2	2331	51

3. 10. AQS CU10 CCU History of Modifications

EC No.	Date	Part Number	Description of Bugs, Changes and Modifications	Ser.No.	New EC – Level
2482	19.6.98	H9503	Introduction of AQS CCU CU10 Layout version H3P2380	0010	00

4. Condensed technical Description

4. 1. Architecture

The CCU is build out of three Units :

- Processor .
- Memory
- L_bus incorporating

  1. The ETHERNET and the Fast–ETHERNET interface, which can be a Master on the L–bus and can access only the Memory.

  2. The VME bus interface, which can be a Master on the L–bus and can access only the Memory.

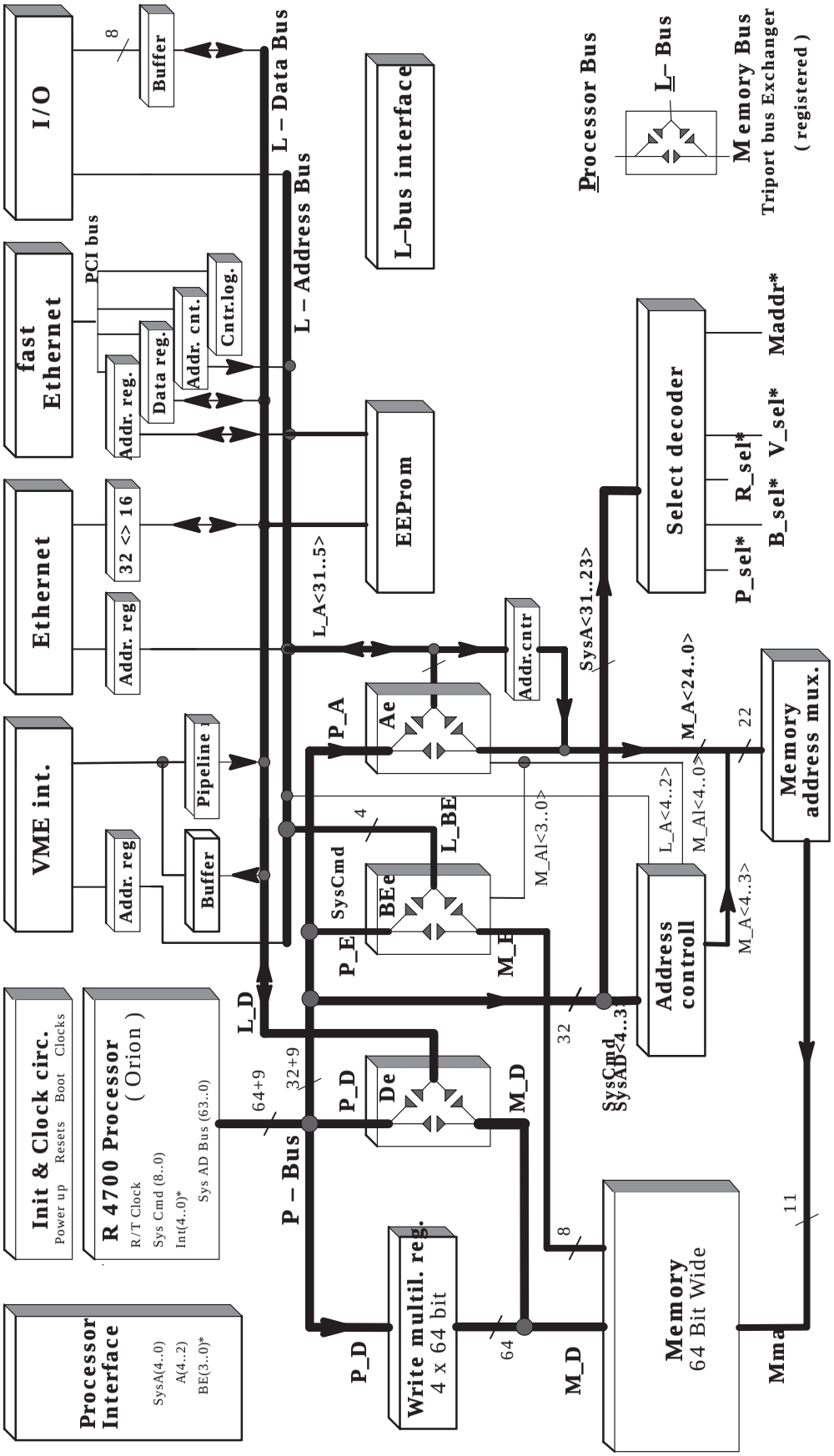
  3. Slave devices which are accessible only by the CPU.

The communication between these Sections is provided by Interconnect Interface. This is a CCU's Internal Interface resolving the arbitration, buffering and interleaving tasks between the Sections. Each Section is attached to the Interconnect by means of Ports. Each Port contains following elements:

- Data exchanger (De)
- Byte Enable exchanger (BEe)
- Address exchanger (Ae)
- Control logic.

4. 1. 1. Block Diagram of CCU

Figure 15: Block diagram CU09/10


I/O
8
Buffer
L – Data Bus
L – Address Bus
L–bus interface
Processor Bus
L– Bus
Memory Bus
Triport bus Exchanger
(registered)
fast Ethernet
PCI bus
Addr. reg.
Data reg.
Addr. cnt.
Cntr.log.
Ethernet
32 <> 16
Addr. reg
EEProm
L_A<31..5>
Select decoder
Maddr*
R_sel*
V_sel*
B_sel*
P_sel*
SysA<31..23>
Addr.cntr
VME int.
Pipeline
Addr. reg
Buffer
P_A
Ae
M_A<24..0>
22
Memory address mux.
4
SysCmd
L_BE
BEe
M_BE
M_Al<3..0>
L_A<4..2>
M_Al<4..0>
Address controll
M_A<4..3>
P_E
L_D
32
SysCmd
SysAD<4..3>
Init & Clock circ.
Power up Resets Boot Clocks
R 4700 Processor
(Orion)
R/T Clock
Sys Cmd (8..0)
Int(4..0)*
Sys AD Bus (63..0)
64+9
32+9
P – Bus
P_D
De
M_D
Processor Interface
SysA(4..0)
A(4..2)
BE(3..0)*
Write multil. reg.
4 x 64 bit
64
8
Memory
64 Bit Wide
11
Mma

4. 2. Logical References to memory and I/O devices

Access Characteristics

- Depending on configuration, the cpu can work in big or little endian mode. For independence the operands within io–device code ranges should be referred to as word (32 bit) operands with the valid bytes indicated by ”b” at ”Byte format” (see below).
- ”Byte 0” means the byte connected to data lines D0 to D7
- Byte, halfword (2 byte), word (4 byte) and block (4 word) accesses are supported
- The cpu reads always 4 bytes at once from the memory range, but it reads from the vme io–code range and it writes to evry location only the bytes which the processor wants to be accessed.

Table 13: CU04 through CU09 predestinate the following address map:

Physical Address	Destination	Access via	Block mode
00000000 to end of onboard DRAM	Main memory	local bus	yes
End of onboard DRAM up to 0FFFFFFF	Main memory	vme bus	yes
10000000 to 17FFFFFF	(former graphic memory)	vme bus	no
18000000 to 1DFFFFFF	Controller memory	vme bus	no
1E000000 to 1EFFFFFF	Device codes	vme bus	no
1F000000 to 1F3FFFFF	CU09/10 onboard io−codes	local bus	no
1F400000 to 1F7FFFFF	CU09/10 onboard Flash RAM	local bus	no
1F800000 to 1FFFFFFF	CU09/10 firmware range	local bus	no
20000000 to FFFFFFFF	main memory	vme bus	yes

4. 2. 1. Firmware

- The reserved firmware range is 8 mbyte.
- The firmware memory is 32 bits wide, containing 2 Mbyte from address 1FC00000 to 1FDFFFFF. It consists of 2 devices, 16 bits wide each.

4. 2. 2. Flash EPROM

- The reserved Flash firmware range is 4 mbyte.
- The Flash memory is 8 bits wide, containing 2 mbyte and is mapped from 1F400000 – 1F5FFFFF address region.
- The Flash memory is the Sector Erase Flash EPROM Am29F016
- The 2 Mbytes of data is divided into 32 sectors of 64 Kbytes and programmed in system.
- The Am29F016 memory features hardware sector group protection disabled by program and divided into eight–four sector groups.: 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31.

4. 2. 3. Onboard memory

It is possible to install 16, 32, or 64 Mbyte DRAM on board. This RAM has to be enabled by setting jumper W3 and is then located in the lowest address space starting with address 0x0. The installed memory volume must be properly selected by setting of jumper W5 (see ”Operational settings”).
Layout version H3P2160B supports up to 64 Mbyte on board DRAM.

4. 2. 4. VME bus port

4. 2. 4. 1. Master Port

Special Features

- In general the cpu provides as bus master the so called **”extended address AM–Code”** indicating the validity of all address lines. But there are two special device code ranges that causes the cpu to escort their bus activities with the **”standard address AM–Code 3D”** or the **”short address AM–Code 2D”**. These ranges are reserved for VME–Devices that are incapable of decoding address lines A24 to A31 (standard) or A16 to A31 (short).
- The interrupt vectors of the vme bus can be read by accessing special vme device codes.

Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1E9xxxxx	Short AM−Code range 2D	R/W	b b b b
1EA00000 to 1EBFFFFF	Standard AM−Code range 3D	R/W	b b b b

Address	Destination	Read/Write	Byte Format 3 2 1 0
1E89xxxx	interrupt vector of IRQ1	R	x x x b
1E8Axxxx	interrupt vector of IRQ2	R	x x x b
1E8Bxxxx	interrupt vector of IRQ3	R	x x x b
1E8Cxxxx	interrupt vector of IRQ4	R	x x x b
1E8Dxxxx	interrupt vector of IRQ5	R	x x x b
1E8Exxxx	interrupt vector of IRQ6	R	x x x b
1E8Fxxxx	interrupt vector of IRQ7	R	x x x b

4. 2. 4. 2. Slave Port

VME bus accesses can reach only the on board DRAM addresses via this port. The address range depends on the installed volume and starts always with VME bus address 0x0.
Byte, word, longword, 2–, 3–, 4–word nibbles and pagemode accesses are possible. Pagemode is not recommended because of its impact to the on board ethernet operation. Single word writes and reads use a single read/write register. A pipeline structure is made for multiple writes and higher bandwidth.
The slave port accepts VME bus references with extended 32–bit addresses escorted with the following AM–Codes:

0F, 0E, 0D, 0B, 09;

4. 2. 5. Ethernet 10BaseT

Notes

- The 10BaseT ethernet subsystem is based on the Am7990 with 32 bit address and a 32 bit wide data port.
- DMA address bits 24 to 31 are clamped to zero.

Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F060xxx	Am7990 Register Data Port	R/W	x x b b
1F061xxx	Am7990 Register Address Port	R/W	x x b b

4. 2. 6. Fast Ethernet 10/100BaseT

Ethernet Controller DEC 21140A

- the chip is connected 32–bit wide to the on board Local bus in case of DMA transfers

- can work in big or little endian mode
- supports byte, word and longword accesses
- supports DMA bursts of up to 32 longwords
- The DEC 21140A Fast Ethernet LAN Controller is mapped into I/O address space.

Configuration Register Device Codes

Address	Destination	Description	Read/ Write	Byte Format 3 2 1 0	Reset Content
1F080000	CFID	Identification	R	bbbb	00091011
1F080004	CFCS	Command and Status	R/W	bbbb	02800000
1F080008	CFRV	Revision	R	bbbb	02000011
1F08000C	CFLT	Latency timer	R/W	bbbb	00000000
1F080010	CBIO	Base I/O address	R/W	bbbb	undefined
1F080014	CBMA	Base memory address	R/W	bbbb	undefined
1F080018	– –	Reserved	R/W	bbbb	
1F080038	– –	Reserved	R/W	bbbb	
1F08003C	CFIT	Interrupt	R/W	bbbb	undefined
1F080040	CFDA	Driver area	R/W	bbbb	undefined

Control and Status Register Device Codes

The CSRs registers are accessibly only after loading a I/O base address (0x1F090000) into CBIO register and by setting I/O space access bit in CFCS register.

Notes

- W: writing is only effective under suspended state

Address	Destination	Description	Read/ Write	Byte Format 3 2 1 0	Reset Content
1F090000	CSR0	Bus Mode	R/W*	bbbb	FF800000
1F090008	CSR1	Transmit poll demand	R/W*	bbbb	FFFFFFFF
1F090010	CSR2	Receive poll demand	R/W*	bbbb	FFFFFFFF
1F090018	CSR3	Receive list base address	R/W*	bbbb	unpredictable
1F090020	CSR4	Transmit list base address	R/W	bbbb	unpredictable
1F090028	CSR5	Status	R/W	bbbb	FC000000
1F090030	CSR6	Operation mode	R/W*	bbbb	32000040
1F090038	CSR7	Interrupt enable	R/W	bbbb	FFFE0000

Address	Destination	Description	Read/ Write	Byte Format 3 2 1 0	Reset Content
1F090040	CSR8	Missed frame counter	R	bbbb	00000000
1F090048	CSR9	Serial ROM and MII manager R/W	R/W	bbbb	FFF097F0
1F090050	CSR10	Reserved		bbbb	undefined
1F090058	CSR11	General–purpose timer	R/W	bbbb	FFFE0000
1F090060	CSR12	General–purpose port	R/W	bbbb	FFFFFEXX
1F090068	CSR13	Reserved		bbbb	undefined
1F090070	CSR14	Reserved		bbbb	undefined
1F090078	CSR15	Watchdog timer	R/W	bbbb	FFFFFEC8

DP83840 Physical Layer

- The chip is a Physical Layer device for Ethernet 10BASE–T and 100BASE–X using category 5 Unshielded, Type 1 Shielded and Fiber Optic cables
- The chip interfaces the PMD sublayer through DP82223 Twisted Pair Transceiver to the MAC layer 21140A through a Media Independent Interface (MII)
- The 32 word–wide MII status and control registers are accessible through the serial management data interface pins MDC and MDIO driven by 21140A via CSR9 register

Physical Layer MII Register allocation

Address	Destination	Description
00h	BMCR	Basic Mode Control Register
01h	BMSR	Basic Mode Status Register
02h	PHYIDR1	PHY Identifier Register #1
03h	PHYIDR2	PHY Identifier Register #2
04h	ANAR	Auto–Negotiation Advertisement Register
05h	ANLPAR	Auto–Negotiation Link Partner Ability Register
06h	ANER	Auto–Negotiation Expansion Register
07h–0fh	––	Reserved
10h–11h	––	Reserved
12h	DCR	Disconnect Counter Register
13h	FCSR	False Carrier Sense Counter Register

Address	Destination	Description
14h	−−	Reserved
15h	RECR	Receive Error Counter Register
16h	SRR	Silicon Revision Register
17h	PCR	PCS Sub−Layer Configuration Register
18h	LBREMR	Loopback,Bypass,Receiver Error Mask Reg.
19h	PAR	Physical Address Register
1Ah	−−	Reserved
1Bh	10BTSR	10BASE−T Status Register
1Ch	10BTCR	10BASE−T Configuration Register
1Dh−1Fh	−−	Reserved

Differences between DP83840 and 83840A

Address	Destination	Bit	DP83840	DP83840A
00h	BMCR	6	Reserved	Management Frame Preamble Suppression indicator selectable
03h	PHYIDR2	3:0	set to 0000	set to 0001
05h	ANLPAR	5	Does not reflect Link Partner 10BASE−T Ability after parallel detection	Reflects Link Partner 10BASE−T Ability after parallel detection
05h	ANLPAR	7	Does not reflect Link Partner 100BASE−T Ability after parallel detection	Reflects Link Partner 100BASE−T Ability after parallel detection
16h	SRR	15:0	set to 0x0000	set to 0x0001
17h	PCR	14	Stream Cipher time−out timer is fixed	Stream Cipher time−out timer is selectable
18h	LBREMR	5	Reserved	Able to disable/enable the TD+/− outputs during 100BASE−T loopback
18h	LBREMR	6	Reserved	Control CSR behavior during Full−duplex operation
18h	LBREMR	15	Does not control Bad SSD code generation	Control Bad SSD code generation

Address	Destination	Bit	DP83840	DP83840A
19h	PAR	7	Unable to determinate the duplex status	Indicate the current duplex status
19h	PAR	8	Reserved	Enable/Disable Far End Fault Indication Protocol
19h	PAR	10	Unable to determinate the ability of Auto−Negotiation	Indicates Auto−Negotiation is enabled
19h	PAR	11	Reserved	Assert/De−assert CRS after descrambler time−out

Differences between DP83840 and 83840A in full duplex mode

Address	Destination	DP83840	DP83840A	Difference
00h	BMCR	0x3100	0x3100	
01h	BMSR	0x782f	0x782f	
02h	PHYIDR1	0x2000	0x2000	
03h	PHYIDR2	0x5c00	0x5c01	Revision Model
04h	ANAR	0x1e1	0x1e1	
05h	ANLPAR	0x1e1	0x41e1	Link Partner ACK
06h	ANER	0x1	0x1	
07h-0fh	−−			
10h-11h	−−			
12h	DCR	undefined	undefined	
13h	FCSR	undefined	undefined	
14h	−−			
15h	RECR	undefined	undefined	
16h	SRR	0x0	0x1	Silicon Revision
17h	PCR	0x8040	0x8060	Carrier Integrity Monitor
18h	LBREMR	0x8004	0x8004	
19h	PAR	0x28	0xca8	DIS_CRS_JAB AN_EN_STAT DUPLEX_STAT
1Ah	−−			

Address	Destination	DP83840	DP83840A	Difference
1Bh	10BTSR	0x0	0x0	
1Ch	10BTCR	0xa3b9	0xa3b9	
1Dh–1Fh	––			

4. 2. 7. RS232 Interface

Notes

- The RS232/RS485 Interfaces reside in six Z85C230 providing 12 separate channels.
- Channel A is intended to be the ”console”, channel B to L to be ”tty01”, ”tty02”,..., ”tty09”,”tty10”,”tty20”
- tty10 and tty20 are configured as RS485 channels
- The frequency of PCLK at pin 23 of Z85C230 is 10 MHz

Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F020xxx	Channel B Control Register, tty01	R/W	x x x b
1F021xxx	Channel B Data Register, tty01	R/W	x x x b
1F022xxx	Channel A Control Register, cons.	R/W	x x x b
1F023xxx	Channel A Data Register, cons.	R/W	x x x b
1F024xxx	Channel D Control Register, tty03	R/W	x x x b
1F025xxx	Channel D Data Register, tty03	R/W	x x x b
1F026xxx	Channel C Control Register, tty02	R/W	x x x b
1F027xxx	Channel C Data Register, tty02	R/W	x x x b
1F030xxx	Channel F Control Register, tty05	R/W	x x x b
1F031xxx	Channel F Data Register, tty05	R/W	x x x b
1F032xxx	Channel E Control Register, tty04	R/W	x x x b
1F033xxx	Channel E Data Register, tty04	R/W	x x x b
1F034xxx	Channel H Control Register, tty07	R/W	x x x b
1F035xxx	Channel H Data Register, tty07	R/W	x x x b
1F036xxx	Channel G Control Register, tty06	R/W	x x x b
1F037xxx	Channel G Data Register, tty06	R/W	x x x b
1F038xxx	Channel J Control Register, tty20	R/W	x x x b

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F039xxx	Channel J Data Register, tty20	R/W	x x x b
1F03Axxx	Channel I Control Register, tty10	R/W	x x x b
1F03Bxxx	Channel I Data Register, tty10	R/W	x x x b
1F03Cxxx	Channel L Control Register, tty9	R/W	x x x b
1F03Dxxx	Channel L Data Register, tty9	R/W	x x x b
1F03Exxx	Channel K Control Register, tty8	R/W	x x x b
1F03Fxxx	Channel K Data Register, tty8	R/W	x x x b

4. 2. 8. JTAG Interface

- The JTAG Interfaces is based on SCANPSC100F National Embedded Boundary Scan Controller.
- It is 8 bits wide parallel interface, and mapped in to 1F0A0000 – 1F0A3FFF address region.
- JTAG submodul is compatible with IEEE 1149.1 JTAG Standard Test Access Port and Boundary Scan Architecture.
- Supported National,s SCAN Ease (Embedded Application Software Enable) Software.
- The frequency of PCLK at pin 25 of SPSC100F is 25 MHz.
- The JTAG_INT source interrupt is ored with all RS_INT interrupts into INT_0 summary interrupt.

JTAG Controller Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F0A0000	TDO Shifter/Buffer	W	– – – x b
1F0A0000	Counter Register 1	R	– – – x b
1F0A0004	TDI Shifter/Buffer	W	– – – x b
1F0A0004	TDI Shifter/Buffer	R	– – – x b
1F0A0008	TMS0 Shifter/Buffer	W	– – – x b
1F0A0008	Counter Register 2	R	– – – x b
1F0A000C	TMS1 Shifter/Buffer	W	– – – x b
1F0A000C	Counter Register 3	R	– – – x b
1F0A0010	32−Bit Counter	W	– – – x b
1F0A0010	Counter Register 0	R	– – – x b

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F0A0014	MODE0	W	– – – x b
1F0A0014	MODE0	R	– – – x b
1F0A0018	MODE1	W	– – – x b
1F0A0018	MODE1	R	– – – x b
1F0A001C	MODE2	W	– – – x b
1F0A001C	MODE2	R	– – – x b

4. 2. 9. Real Time Clock and NVRAM

Notes

- The MK48T02 of SGS–Thomson is installed to implement these two functions by one device.
- It is a 2K–Byte–Static–RAM with its eight upmost cells being reserved as hold register for the real time clock information.
- The lower half of the 2 kbyte is normally protected and can only be written by means of the special PAL device ”CU09Nx01 ” of the service staff. So far, this range contains only the ”ethernet physical address”.
- Besides the timing registers, the upper half of NVRAM contains all the other boot parameters read with ”printenv” and changed with ”setenv” in the monitor program.

Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F00000x to 1F006FFx	NVRAM range, lower half	R	x x x b
1F00700x to 1F007F7x	NVRAM range, upper half	R/W	x x x b
1F007F8x	Control Register	R/W	x x x b
1F007F9x	Seconds	R/W	x x x b
1F007FAx	Minutes	R/W	x x x b
1F007FBx	Hour	R/W	x x x b
1F007FCx	Day	R/W	x x x b
1F007FDx	Date	R/W	x x x b

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F007FEx	Month	R/W	x x x b
1F007FFx	Year	R/W	x x x b

4. 2. 10. Configuration and Status Register

Notes

- There are 4 configuration register and 1 status register. Each of them is 8 bit wide.
- Each configuration register provides two hexadecimal digits indicating the version of two individual onboard subsystems as follows:

CPU version	CPUV = 0x9 on CU09
Processor version	PRZV = 0x1
Real Time Clock version	RTCV = 0x1
Keyboard Controller version	KBV = 0x0
RS232 Interface version	RSV = 0x2
Ethernet version	ETHV = 0x1 on CU05−CU08 ETHV = 0x2 for CU09 with10/100BASE−T only ETHV = 0x3 for CU09 with 10BASE2 and 10/100BASE−T
SCSI Controller version	SCSIV = 0x0

A subsystem is not available if the respective digit equals to zero. All configuration register outputs are provided in their negated form

The **STATUS register** accommodates the temperature and VME bus time out status bits, 4 LED bits and 3 control bits of the ”CIS” channel (component identification system).

Read access to the STATUS register provides the occurrence of TMP_INT (temperature interrupt) on bit 1 and the occurrence of vme bus time out on bit 0 since last read. Both are low active and cleared in sequence of a read. Bit 3 of the status reflects the state of SDA, this is the serial data line of the VME–Bus.

Write access stores the upper 4 bits (D7,...,D4) of the transferred byte to the 4Bit–Led–Register. D3, D2 and D1 control the serial bus lines SDA, SCLK and ACLK.

	Bit Allocation of the STATUS Register							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write	Leftmost LED	LED at front edge		Right-most LED	SDA at J1/B22	SCLK at J1/B21	ACLK at J2/B3	
Read							TMP_INT	VME bus Time out

Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F05Fxxx	STATUS	R/W	x x x b
1F050xxx	SCSIV, −−	R	x x x b
1F051xxx	RSV, ETHV	R	x x x b
1F052xxx	RTCV, KBV	R	x x x b
1F053xxx	CPUV, PRZV	R	x x x b

4. 2. 11. Interrupt Router

Notes

- The processor reaches its 6 interrupt levels by means of the 6 interrupt inputs, INT_5..INT_0.
- INT_5 (highest level) is assigned and hardwired to the floating point interrupt.
- The router distributes all onboard and vme bus interrupt sources to level 0 to 4. Source interrupts intended to a certain level are ored to produce the processor interrupt INT_i. The source interrupts of each level form an Interrupt Register that can be read via device code providing the status of that level.
- Once activated a source interrupt signal has to keep its level up to being acknowledged with a special activity like reading an assigned status register or the assigned vme interrupt vector.
- The router contains only for the temperature interrupt ”TMP_INT” an interrupt mask. This mask is opened after reset and by writing to the device code with D1=1 and closed by writing with D1=0.

Routed Source Interrupts

IRQ1..7	7 VME bus interrupts
RS_INT0..5	5 interrupts of 5 individual RS232 subsystems
	RS_INT0 is the output of Z85C230, Channel A and B

	RS_INT1 is interrupt of Channel C and D
	RS_INT2 is interrupt of Channel E and F
	RS_INT3 is interrupt of Channel G and H
	RS_INT4 is interrupt of Channel I and J
	RS_INT5 is the output of Z85C230, Channel K and L
JTAG_INT	JTAG interrupt, connected to pin 19 of the SCANPCS100F
CAN_INT	CAN interrupt, connected to pin 16 of the SJA1000
TMP_INT	High Temperature interrupt
LAN_INT	Ethernet Interrupt, pin 6 of Am7990
F_INT	Fast Ethernet Interrupt, pin 1 of the DEC 21140A
LINK_INT	Fast Ethernet Link Interrupt, pin 38 of the DP83840A

The routed distribution of source interrupts and their location in the corresponding interrupt register are as follows:

Interrupt Level INT_0	INT_1	INT_2	INT_3	INT_4	Location in Reg.
IRQ1	IRQ4	IRQ6	0	IRQ7	D0
TMP_INT	IRQ3	IRQ5	0	F_INT	D1
res TIM_INT1	IRQ2	0	0	LINK_INT	D2
0	0	0	0	res FDDI	D3
0	0	0	0	res FDDI	D4
0	0	0	0	res FDDI	D5
0	0	0	0	res FDDI	D6
RS_INT	0	0	res TIM_INT0	LAN_INT	D7

Notes:

- RS_INT is the ored sum of RS_INT0,...,RS_INT5, JTAG_INT and CAN_INT
- Bits 2 to 6 of INT_4 are reserved for FDDI source interrupts.
- Bits 2 of INT_0 and 7 of INT_3 are reserved for DP8571A Timer source interrupts.
- Bit 0 of INT_4 is a VME–bus interrupt .7
- Bit 7 of INT_4 is a 10Mb/s Am7990 Ethernet Controller interrupt.

Device Codes

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F040xxx	INT0 Register	R	x x x b
1F041xxx	INT1 Register	R	x x x b

Address	Destination	Read/Write	Byte Format 3 2 1 0
1F042xxx	INT2 Register	R	x x x b
1F043xxx	INT3 Register	R	x x x b
1F044xxx	INT4 Register	R	x x x b
1F048xxx	INT0 Mask (only D1 implemented)	W	x x x b

4. 2. 12. CIS access

The information EEPROM of the Component Identification System is connected to the CCU controlled CIS channel. The EEPROM of all CCU's have one and the same unique address out of all possible channel addresses as follows:

Device	SBA binary										SBA hex	
	9	8	7	6	5	4	3	2	1	0	old	new
	Protocol bit	Group address						EEPROM address				
CCU	0	0	0	0	0	0	1	0	0	0	008	010