

# VME Backplane 8-Slot

**AQS**  
**Technical Manual**

**Version 001**

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**BRUKER**

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## ***AQS VME Backplane, 8–Slot***

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## 1. Starting with VB8

### 1. 1. Special features

- This backpanel provides space for 8 VME based devices of 4 TE
- Slot 1 (the leftmost one, seen in plug-in direction of the AQ devices) is the host processor slot (CCU10). Only in this slot the CCU can correct work and route their RS485 signals to connector X3
- Slot 2 through 8 can be used for AQ devices (TCU3, FCU3, RCU, GCU) only.
- No jumpers have to be set to connect daisy chain signals over free slots.
- The backplane is assembled with an adapter pcb which allows the use of a plug-in power supply from the rear side.
- Instead of the former used 30-pin connector in the middle position of each slot this backplane uses a 90-pin connector (J0) housing the special AQ-Buses and configuration signals.

### 1. 2. Hardware Implementation

The new features of this backpanel require some handling rules to be considered

- Only devices with the proper J0 90-pin connector (CU10, TCU3, FCU3) or devices without any connector in the middle position (RCU, GCU) should be inserted.
- Violently inserting of elder devices with 30-pin connectors could damage this backpanel.
- Slot 1 is allocated only for the CCU. Slots 2 to 8 are allocated only for AQ devices.
- TCU3 should be the leftmost one of the AQ devices.
- The configuration signals at J0 make auto configuration schemes possible.

This is used on FCU3. See the following:

#### 1. 2. 1. Auto-Configuration of FCU3

Four FCU3 boards can be combined to provide 8 Frequency Channels called "FCU Channel 1" to "FCU Channel 8".

Creating a special channel pair needs no jumper setting. FCU3 is provided with a self configuring scheme which works as follows:

##### Configuration Scheme

1. Each Channel A becomes the odd channel and each Channel B the even one.
2. The leftmost FCU3 (looking at the front side) configures itself to be FCU Channel 1 and 2. A FCU3 in the next position at their right side will be FCU Channel 3 and 4 and so forth.

3. Gaps or other devices between FCU3 lead to a second Channel 1/2 pair and to malfunctioning and should be avoided.  
If any reason would necessitate gaps between FCU's, jumpers are provided on FCU3 (W15) which can override the configuration scheme.

## 2. Specifications

### 2.1. Versions

Up to now, Nov. 1999, 3 versions of the backplane, called "Rev.00, 01 and 02" have been in use. Rev.00 has been assembled only in the first 25 prototypes. Rev.01 and 02 are functionally identical and used for production. Rev.01 needs a wire between J0–E3 of any slot and X3 pin 8. Rev.02 has this connection included in its pcb layout.

Rev.00 needs this wire too which connects the "SGU Reset" of the TCU3 through X3 to the SGU backplane.

The revision level is seen in plug-in direction of the boards at the left side down beneath the label "X201" of slot 1.

Version	Differences to Rev.02	Consequence	Requirements
Rev.00	Signal Jext not implemented	Inconsiderable for any application	SGU Reset function needs a wire between J0–E3 of any slot and X3 pin 8
	No termination resistors at TCLK	JTAG programming by CCU not possible	
	Power Supply Adapter not mountable	Power Supply has to be connected by cable	SGU Reset function needs a TCU3 with $EC \geq 01$
Rev.01	J0–E3 and X3 pin 8 connected by wire	No restrictions	SGU Reset function needs a TCU3 with $EC \geq 01$
Rev.02			

### 2.2. Construction

VB8 is a Standard 64-bit VME Bus backplane equipped with 32-bit VME Bus connectors J1 and J2 and application specific buses at an additional 90-pin connector J0.

#### Power Adapter

A power adapter pcb board is assembled at the rear side making it possible to use a plug-in power supply.

The power supply is unable to deliver 3,3 –Volt current. Therefore the power adapter provides also the possibility to assemble a DC/DC Converter supplying 8 A current of 3,3 V made from 5 V. So far the adapter is not equipped with this converter. Making low voltage current where it is used provides greater flexibility.

#### Locking Plate

A Locking Plate is assembled tight to J0 which is to prevent insertion of AQS devices with 30-pin connector as J0.

#### Connectors on the Backplane

The connectors of VB8 provide the following:

**J1 and J2**

- Standard 32-bit VME Bus signals, slot 1 to 8
- Real time AQ Bus signals, slot 2 to 8
- Y Bus signals, slot 2 to 8

**J0**

- Fast AQ Bus control signals, slot 2 to 8
- F Bus signals, slot 2 to 8
- SGU Reset signal, slot 1 to 8
- JTAG Bus for programming and testing, slot 1 to 8
- BBIS channel, slot 1 to 8
- RS485 signals to X3, slot 1
- Daisy-chain signals for auto configuration, slot 1 to 8
- Reserved clock lines, slot 1 to 8

**X3 (Rear side)**

- RS485 signals to SGU backplane
- SGU Reset signal to SGU backplane

**Connectors on the Power Adapter (Rear side)****XA1**

- Power connector of the Power Supply

**XA2**

- Fan power

**XA3, XA4**

- 5 Volt and GND to the SGU backpanel



**Backplane Drawings**

Figure 1: Front View at the Backplane

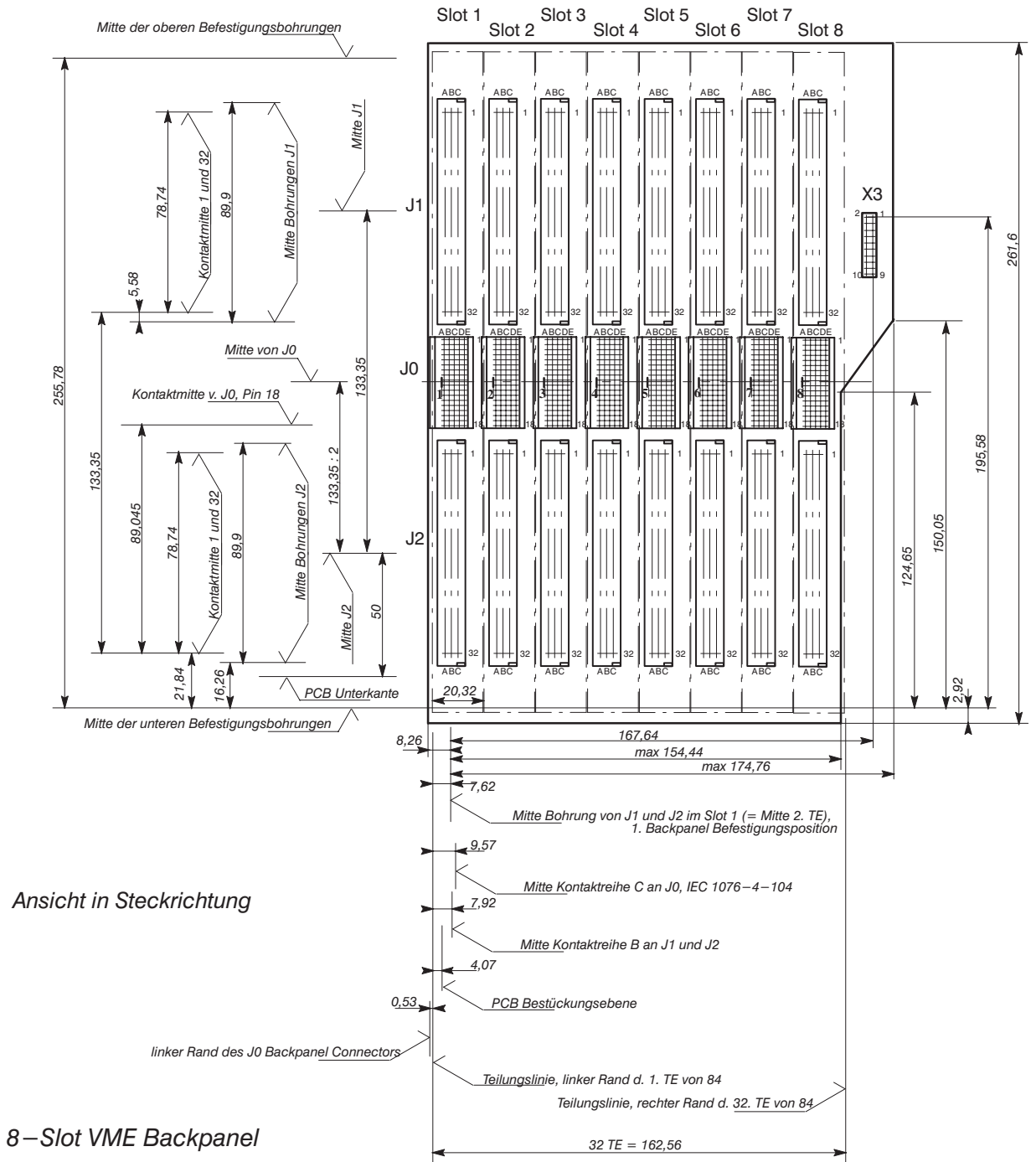
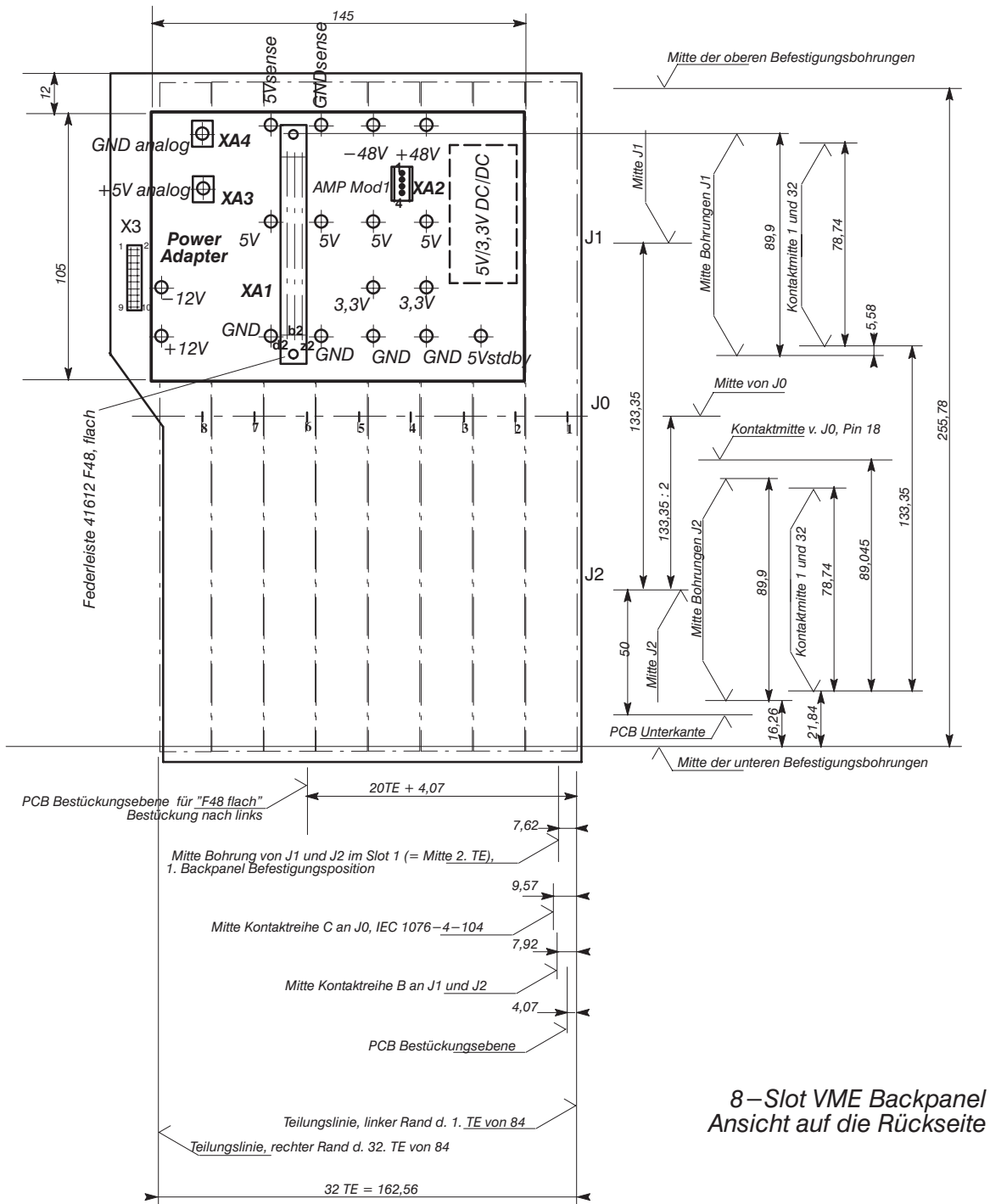


Figure 2: Rear View at Backplane and Power Adapter



8-Slot VME Backpanel Ansicht auf die Rückseite

### 2. 3. Part numbers

Assembly	Parts	Part#
H9578	AQS VME Backplane	H9443
	AQS VME PS_Adapter (Power Supply Adapter)	H9510
	AQS Motherboard. Steckschutz (Locking plate)	HZ06631

## 2. 4. Operational Settings

The assembly needs no configurations or jumper settings.

## 2. 5. Connectors and Signal Allocations

### 2. 5. 1. J2, rows A + C

Pins of Slot 1 are left open. Slot 2 to 8 are identical allocated.

	Slot 2 to 7		Slot 8			
	Row A	Row C	Term	Row A	Row C	Term
1	AQA_0	AQI_0	Pd	AQA_0	AQI_0	St
2	AQA_1	AQI_1	Pd	AQA_1	AQI_1	St
3	AQA_2	AQI_2	Pd	AQA_2	AQI_2	St
4	AQA_3	AQI_3	Pd	AQA_3	AQI_3	St
5	AQS_0	AQI_4	Pd	AQS_0	AQI_4	St
6	AQS_1	AQI_5	Pd	AQS_1	AQI_5	St
7	AQS_2	AQI_6	Pd	AQS_2	AQI_6	St
8	AQS_3	AQI_7	Pd	AQS_3	AQI_7	St
9	GND_1	GND_6		GND_1	GND_6	
10	AQD_0	AQY_0	Pd	AQD_0	AQY_0	Pd
11	AQD_1	AQY_1	Pd	AQD_1	AQY_1	Pd
12	AQD_2	AQY_2	Pd	AQD_2	AQY_2	Pd
13	AQD_3	AQY_3	Pd	AQD_3	AQY_3	Pd
14	AQD_4	AQY_4	Pd	AQD_4	AQY_4	Pd
15	AQD_5	AQY_5	Pd	AQD_5	AQY_5	Pd
16	AQD_6	AQY_6	Pd	AQD_6	AQY_6	Pd
17	AQD_7	AQY_7	Pd	AQD_7	AQY_7	Pd
18	GND_2	GND_7		GND_2	GND_7	
19	AQY_WR	AQY_AS	Pd	AQY_WR	AQY_AS	Pd
20	AQY_ACK	AQY_DS	Pd	AQY_ACK	AQY_DS	Pd
21	GND_3	GND_8		GND_3	GND_8	
22	AQD_8	res_1	Pd	AQD_8	res_1	Pd
23	AQD_9	res_2	Pd	AQD_9	res_2	Pd
24	AQD_10	res_3	Pd	AQD_10	res_3	Pd
25	AQD_11	res_4	Pd	AQD_11	res_4	Pd
26	AQD_12	res_5	Pd	AQD_12	res_5	Pd
27	AQD_13	res_6	Pd	AQD_13	res_6	Pd
28	AQD_14	res_7	Pd	AQD_14	res_7	Pd
29	AQD_15	res_8	Pd	AQD_15	res_8	Pd
30	GND_4	res_9		GND_4	res_9	Pd
31	GND_5	GND_9		GND_5	GND_9	
32	AQ_ST	AQ_EXE_J2	Pd	AQ_ST	AQ_EXE_J2	Pd

### Termination

Only at Slot 8

St Attenuator with 470 Ohm to +5 Volt and 680 Ohm to GND

Pd Pull-down resistor 470 Ohm to GND

## 2. 5. 2. J0, rows A , B, C, D, E

### Signal allocation at Slot 1

	Row A	Row B	Row C	Row D	Row E
1	Jext	TCLK	TMS	TDI	TDO
2	GND	GND	ACLK	SCLK	SDA
3	res_Ltg_4	res_Ltg_3	res_Ltg_2	res_Ltg_1	SGU Reset
4	GND	GND	GND	GND	GND
5	3,3V	3,3V	3,3V	3,3V	3,3V
6	res_CLK_4	res_CLK_3	res_CLK_2	res_CLK_1	res_CLK_0
7	GND	GND	GND	GND	GND
8					
9					
10					
11					
12					
13	DC6_out	DC4_out	DC2_out	DC0_out	
14	DC7_out	DC5_out	DC3_out	DC1_out	
15	+12V	WUP_1	GND	RxD+_1	TxD+_1
16				RxD-_1	TxD-_1
17	+12V	WUP_2	GND	RxD+_2	TxD+_2
18	GND	GND	GND	RxD-_2	TxD-_2

### Signals with identical allocation at Slot 2 to 8

	Row A	Term . an Slot	Row B	Term . an Slot	Row C	Term . an Slot	Row D	Term . an Slot	Row E	Term . an Slot
1	Jext		TCLK	St1 1 +8	TMS		TDI		TDO	
2	GND		GND		ACLK	St3; 8	SCLK	St3; 8	SDA	
3	res_Ltg_4	St1; 1+8	res_Ltg_3	St1; 1+8	res_Ltg_2	St1; 1+8	res_Ltg_1	St1; 1+8	SGU Reset	St1; 1+8
4	GND		GND		GND		GND		GND	
5	3,3V		3,3V		3,3V		3,3V		3,3V	
6	res_CLK_4	St2; 1+8	res_CLK_3	St2; 1+8	res_CLK_2	St2; 1+8	res_CLK_1	St2; 1+8	res_CLK_0	St2; 1+8
7	GND		GND		GND		GND		GND	
8	FD_0	St1; 2+8	FD_1	St1; 2+8	FD_2	St1; 2+8	FD_3	St1; 2+8	FD_4	St1; 2+8
9	FD_5	St1; 2+8	FD_6	St1; 2+8	FD_7	St1; 2+8	FD_8	St1; 2+8	FD_9	St1; 2+8
10	FD_10	St1; 2+8	FD_11	St1; 2+8	FD_12	St1; 2+8	FD_13	St1; 2+8	FD_14	St1; 2+8
11	FD_15	St1; 2+8	FD_16	St1; 2+8	FD_17	St1; 2+8	FD_18	St1; 2+8	FD_19	St1; 2+8
12	FD_20	St1; 2+8	FD_21	St1; 2+8	FD_22	St1; 2+8	FD_23	St1; 2+8	FD_24	St1; 2+8

	Row A	Termination Slot	Row B	Termination Slot	Row C	Termination Slot	Row D	Termination Slot	Row E	Termination Slot
13	FD_25	St1; 2+8	FD_26	St1; 2+8	FD_27	St1; 2+8	FD_28	St1; 2+8	FD_29	St1; 2+8
14									FD_30	St1; 2+8
15									FD_31	St1; 2+8
16									F_REQ	St1; 2+8
17									GND	
18							AQ_EXE_J 0	Pd; 8	AQ_STROB E_B	Pd; 8

### Termination

- St1 Attenuator with 330 Ohm to +5 Volt and 470 Ohm to GND
- St2 Attenuator with 220 Ohm to +5 Volt and 330 Ohm to GND
- St3 Attenuator with 470 Ohm to +5 Volt and 680 Ohm to GND
- Pd Pull-down resistor 470 Ohm an GND

### Signals with slot dependent allocation

Not terminated

Contact	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8
D13	1_DC0_out							
D14	1_DC1_out	2_DC0_out	3_DC0_out	4_DC0_out	5_DC0_out	6_DC0_out	7_DC0_out	
D15		1_DC0_out	2_DC0_out	3_DC0_out	4_DC0_out	5_DC0_out	6_DC0_out	7_DC0_out
D16		2_DC1_out	3_DC1_out	4_DC1_out	5_DC1_out	6_DC1_out	7_DC1_out	
D17		1_DC1_out	2_DC1_out	3_DC1_out	4_DC1_out	5_DC1_out	6_DC1_out	7_DC1_out
C13	1_DC2_out							
C14	1_DC3_out	2_DC2_out	3_DC2_out	4_DC2_out	5_DC2_out	6_DC2_out	7_DC2_out	
C15		1_DC2_out	2_DC2_out	3_DC2_out	4_DC2_out	5_DC2_out	6_DC2_out	7_DC2_out
C16		2_DC3_out	3_DC3_out	4_DC3_out	5_DC3_out	6_DC3_out	7_DC3_out	
C17		1_DC3_out	2_DC3_out	3_DC3_out	4_DC3_out	5_DC3_out	6_DC3_out	7_DC3_out
B13	1_DC4_out							
B14	1_DC5_out	2_DC4_out	3_DC4_out	4_DC4_out	5_DC4_out	6_DC4_out	7_DC4_out	
B15		1_DC4_out	2_DC4_out	3_DC4_out	4_DC4_out	5_DC4_out	6_DC4_out	7_DC4_out
B16		2_DC5_out	3_DC5_out	4_DC5_out	5_DC5_out	6_DC5_out	7_DC5_out	
B17		1_DC5_out	2_DC5_out	3_DC5_out	4_DC5_out	5_DC5_out	6_DC5_out	7_DC5_out
A13	1_DC6_out							
A14	1_DC7_out	2_DC6_out	3_DC6_out	4_DC6_out	5_DC6_out	6_DC6_out	7_DC6_out	
A15		1_DC6_out	2_DC6_out	3_DC6_out	4_DC6_out	5_DC6_out	6_DC6_out	7_DC6_out
A16		2_DC7_out	3_DC7_out	4_DC7_out	5_DC7_out	6_DC7_out	7_DC7_out	
A17		1_DC7_out	2_DC7_out	3_DC7_out	4_DC7_out	5_DC7_out	6_DC7_out	7_DC7_out
A18	GND		GND		GND		GND	

Contact	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8
B18	GND	GND			GND	GND		
C18	GND	GND	GND	GND				

### 2. 5. 3. Signal allocation at X3

	Signal		Signal
2	TxD-_1	1	TxD+_1
4	GND	3	GND
6	RxD-_1	5	RxD+_1
8	SGU Reset	7	WUP_1
10	+12V	9	+12V
12	+12V	11	+12V
14		13	WUP_2
16	RxD-_2	15	RxD+_2
18	GND	17	GND
20	TxD-_2	19	TxD+_2

### 2. 5. 4. Pin Assignment of XA1 to XA4 on the Power Supply Adapter

Pin	XA1, Row z	Current A	XA1, Row b	Current A	XA1, Row d	Current A	XA2	Current A	XA3	Current A	XA4	Current A
1							GND	3	5V analog	14	GND analog	14
2	GND	4	GND	4	GND	4	GND	3				
3							+12V	3				
4	GND	4	GND	4	GND	4	+12V	3				
6	GND	4	GND	4	GND	4						
8	GND	4	GND	4	GND	4						
10	GND sense		GND	4	GND	4						
12	GND	4	GND	4	GND	4						
14	GND	4	+12V	4	+12V	4						
16	-12V	4			+12V	4						
18	5V	4	5V	4	5V	4						
20	5V	4	5V	4	5V	4						
22	5V	4	5V	4	5V	4						
24	5V	4	5V	4	5V	4						
26	5Vsense		5V	4	5V	4						
28	GND analog	4	GND analog	4	GND analog	4						
30	GND analog	4			5V analog	4						
32	5V analog	4	5V analog	4	5V analog	4						

## 2. 6. Power Requirements

The backplane requires the following currents:

	Part-No.	+5 V	+12 V	-12 V	+3,3V J0: A5, B5, C5, D5, E5
VB8	H9578	1,8A	0	0	0

## 3. Service Information

### 3. 1. Operating Conditions

(see also Chapter 1.)

The new features of this backpanel require some handling rules to be considered

- Only devices with the proper J0 90–pin connector (CU10, TCU3, FCU3) or devices without any connector in the middle position (RCU, GCU) should be inserted.
- Violently inserting of elder devices with 30–pin connectors could damage this backpanel.
- Slot 1 is allocated only for the CCU. Slots 2 to 8 are allocated only for AQ devices.
- TCU3 should be the leftmost one of the AQ devices.
- No jumpers have to be set to connect daisy chain signals over free slots.
- The configuration signals at J0 make auto configuration schemes possible.

This is used on FCU3. See the following:

#### 3. 1. 1. Auto–Configuration of FCU3

Four FCU3 boards can be combined to provide 8 Frequency Channels called "FCU Channel 1" to "FCU Channel 8".

Creating a special channel pair needs no jumper setting. FCU3 is provided with a self configuring scheme which works as follows:

##### Configuration Scheme

1. Each Channel A becomes the odd channel and each Channel B the even one.
2. The leftmost FCU3 (looking at the front side) configures itself to be FCU Channel 1 and 2. A FCU3 in the next position at their right side will be FCU Channel 3 and 4 and so forth.
3. Gaps or other devices between FCU3 lead to a second Channel 1/2 pair and to malfunctioning and should be avoided.  
If any reason would necessitate gaps between FCU's, jumpers are provided on FCU3 (W15) which can override the configuration scheme.

### 3. 2. Introduced Versions

Up to now, Nov. 1999, 3 versions of the backplane, called "Rev.00, 01 and 02" have been in use. Rev.00 has been assembled only in the first 25 prototypes. Rev.01 and 02 are functionally identical and used for production. Rev.01 needs a wire between J0–E3 of any slot and X3 pin 8. Rev.02 has this connection included in its pcb layout.

Rev.00 needs this wire too which connects the "SGU Reset" of the TCU3 through X3 to the SGU backplane.



The revision level is seen in plug-in direction of the boards at the left side down beneath the label "X201" of slot 1.

Version	Differences to Rev.02	Consequence	Requirements
Rev.00	Signal Jext not implemented	Inconsiderable for any application	SGU Reset function needs a wire between J0–E3 of any slot and X3 pin 8
	No termination resistors at TCLK	JTAG programming by CCU not possible	
	Power Supply Adapter not mountable	Power Supply has to be connected by cable	SGU Reset function needs a TCU3 with $EC \geq 01$
Rev.01	J0–E3 and X3 pin 8 connected by wire	No restrictions	SGU Reset function needs a TCU3 with $EC \geq 01$
Rev.02			

### 3. 3. History of Modifications

#### AQS VME Backpanel

EC No.	Date	Part Number	Description of Bugs, Changes and Modifications	Ser.No.	New EC–Level
		H9443	Introduction of AQS VME Backpanel Rev.01		00
		H9443	Introduction of AQS VME Backpanel Rev.02, Layout correction, only removing wire patches		01

#### AQS VME Power Supply Adapter

EC No.	Date	Part Number	Description of Bugs, Changes and Modifications	Ser.No.	New EC–Level
		H9510	Introduction of the AQS VME PS Adapter		00